CML Microcircuits
COMMUNICATION SEMICONDUCTORS

CMX7031/CMX7041
AX.25 Modem

D/7031/7041_FI-4.x/5 January 2013

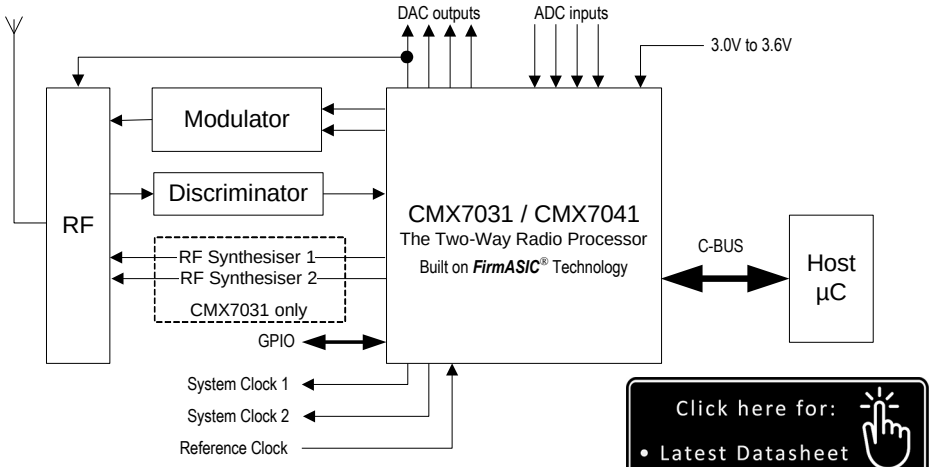
DATASHEET

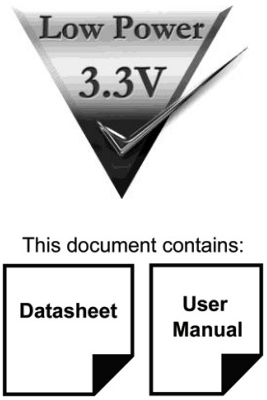
Advance Information

7031/7041FI-4.x: AX.25 Modem (1200bps AFSK and 9600bps GMSK) with Auxiliary System Clocks, ADCs and DACs for use in Amateur Packet Radio

Features

- **1200bps AFSK Modem**
- **9600bps GMSK Modem**
- **Two RF Synthesisers (CMX7031 only)**
- **DTMF Transmit**
- **19.2MHz or 12.4MHz Reference Clock**
- **Available in 64-pin and 48-pin LQFP and VQFN Packages**
- **C-BUS Serial Interface to Host µController**
- **Three Analogue Inputs**
- **NRZI Encoding/Decoding**
- **9600bps Data Scrambler/Descrambler**
- **Transmit pre-emphasis**
- **Two Auxiliary ADCs with Four Mux Inputs**
- **Four Auxiliary DACs**
- **Auxiliary System Clock Outputs**
- **Tx Outputs for Single, Two-Point Modulation**
- **Low-power (3.0V to 3.6V) Operation**
- **Flexible Powersave Modes**





1 Brief Description

The 7031/7041FI-4.x is a full-function, half-duplex, signalling/data processor IC. This makes it a suitable device for both the Data Radio (M2M) and Amateur Packet Radio markets.

The Function Image™ provides a dual wireless data modem function incorporating a 1200bps AFSK modem and a 9600bps GMSK modem. In receive, simultaneous detection of 1200bps AFSK or 9600bps GMSK data is performed and subsequently, demodulation and decoding of the detected format.

The device utilises CML's proprietary *FirmASIC*® component technology. On-chip sub-systems are configured by a Function Image™: this is a data file that is uploaded during device initialisation and defines the device's function and feature set. The Function Image™ can be loaded automatically from an external serial memory or from a host µController over the built-in C-BUS serial interface. The device's functions and features can be enhanced by subsequent Function Image™ releases, facilitating in-the-field upgrades. This document refers specifically to the features provided by Function Image™ 4.x.

Continued…

The CMX7031 features two on-chip RF synthesisers, with easy Rx/Tx frequency changeover, and programmable system clocks to minimise chip count in the final application.

The CMX7041 is identical in functionality to the CMX7031 with the exception that the two on-chip RF Synthesisers have been deleted, which enables it to be supplied in a smaller package.
Other features include two auxiliary ADC channels with four selectable inputs and up to four auxiliary DAC interfaces (with an optional RAMDAC on the first DAC output, to facilitate transmitter power ramping).

The device has flexible powersaving modes and is available in both LQFP and VQFN packages.

Note that text shown in pale grey indicates features that will be supported in future versions of the device.
This Datasheet is the first part of a two-part document comprising a Datasheet and a User Manual: the combined Datasheet/User Manual document and the Function Image™ can be obtained by registering your interest in these products with your local CML representative.

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It is always recommended that you check for the latest product datasheet version from the Datasheets page of the CML website: [www.cmlmicro.com].

1.1 History

Version	Changes	Date
5	• Document released for general use • Figure 1, Block Diagram modified to show scrambler/descrambler for GMSK and Tx pre-emphasis • Section 9.1, C-BUS Register table added to User Manual.	Jan 2013
4	Clarification of reset mechanisms and FI loading. Phase Noise respecified.	June 2011
3	• AuxADC averaging implemented • Figures updated • Corrected GMSK mode sync detect to 24 bits • Added note for 1 bit error allowed during sync detection • Add note on Data Famine • Corrected scrambler figure	Jan 2011
2	• Editorial corrections to match company style • Added GMSK modulation figure	Jan 2011
1	• Original document.	Dec 2010

This is Advance Information; changes and additions may be made to this specification. Parameters marked TBD or left blank will be included in later issues. Items that are highlighted or greyed out should be ignored. These will be clarified in later issues of this document. Information in this advance document should not be relied upon for final product design.

2 Block Diagram

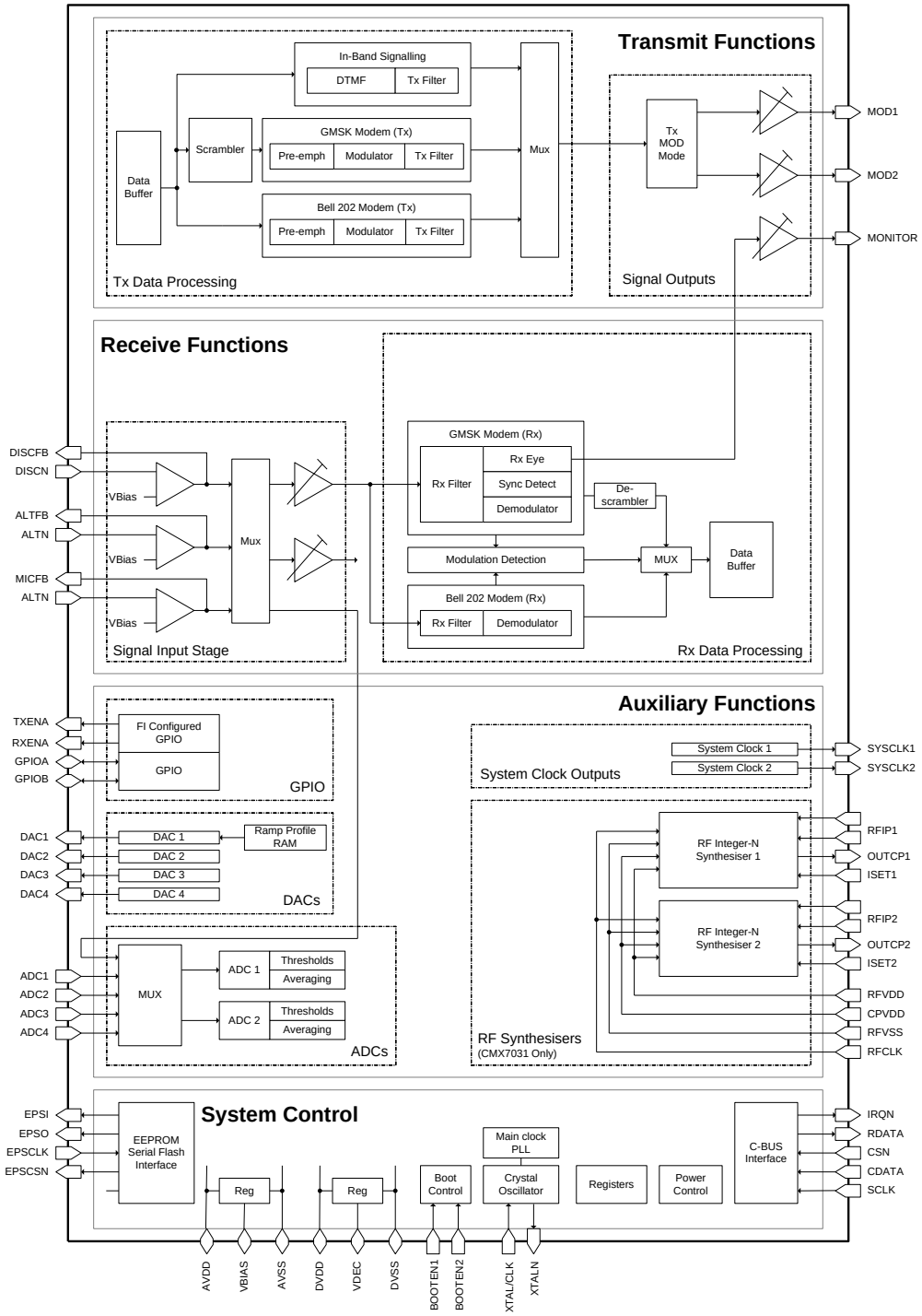


Figure 1 Block Diagram

3 Signal List

CMX7031 64-pin Q1/L9	CMX7041 48-pin Q3/L4	Signal Name	Type	Description
1	**8**	IRQN	OP	C-BUS: A 'wire-ORable' output for connection to the Interrupt Request input of the host. Pulled down to DV_{SS} when active and is high impedance when inactive. An external pull-up resistor (R1) is required.
2	-	RF1N	IP	RF Synthesiser #1 Negative input.
3	-	RF1P	IP	RF Synthesiser #1 Positive input.
4	-	RFVSS	PWR	The negative supply rail (ground) for the 1st RF synthesiser.
5	-	CP1OUT	OP	1st Charge Pump output.
6	-	ISET1	IP	1st Charge Pump Current Set input.
7	-	RFVDD	PWR	The 2.5V positive supply rail for the RF synthesisers. This should be decoupled to RFV_{SS} by a capacitor mounted close to the device pins.
8	-	RF2N	IP	RF Synthesiser #2 Negative input.
9	-	RF2P	IP	RF Synthesiser #2 Positive input.
10	-	RFVSS	PWR	The negative supply rail (ground) for the 2nd RF synthesiser.
11	-	CP2OUT	OP	2nd Charge Pump output.
12	-	ISET2	IP	2nd Charge Pump Current Set input.
13	-	CPVDD	PWR	The 3.3V positive supply rail for the RF charge pumps. This should be decoupled to RFV_{SS} by a capacitor mounted close to the device pins.
14	-	RFCLK	IP	RF Clock Input (common to both synthesisers)[1].
15	-	GPIOA	IP/OP	General Purpose I/O pin (CMX7031 only).
16	-	GPIOB	IP/OP	General Purpose I/O pin (CMX7031 only).
17	-	-	NC	Reserved – do not connect this pin.
18	**9**	VDEC	PWR	Internally generated 2.5V digital supply voltage. Must be decoupled to DV_{SS} by capacitors mounted close to the device pins. No other connections allowed, except for optional connection to RFV_{DD}.
19	**10**	RXENA	OP	Rx Enable – active low when in Rx mode ($C1:b0 = 1).
-	**11**	GPIOA	IP/OP	General Purpose I/O pin (CMX7041 only).
-	**12**	GPIOB	IP/OP	General Purpose I/O pin (CMX7041 only).
20	**13**	SYSCLK1	OP	Synthesised Digital System Clock Output 1.
21	**14**	DVSS	PWR	Digital Ground.
22	-	-	NC	Reserved – do not connect this pin.
23	**15**	TXENA	OP	Tx Enable – active low when in Tx mode ($C1:b1 = 1)
24	**16**	DISCN	IP	Channel 1 inverting input.
25	**17**	DISCFB	OP	Channel 1 input amplifier feedback.

[1] To minimise crosstalk, this signal should be connected to the same clock source as XTAL/CLOCK input.

CMX7031 64-pin Q1/L9	CMX7041 48-pin Q3/L4	Signal Name	Type	Description	
26	**18**	ALTN	IP	Channel 2 inverting input.	
27	**19**	ALTFB	OP	Channel 2 input amplifier feedback.	
28	**20**	MICFB	OP	Channel 3 input amplifier feedback.	
29	**21**	MICN	IP	Channel 3 inverting input.	
30	**22**	AVSS	PWR	Analogue Ground.	
31	**23**	MOD1	OP	Modulator 1 output.	
32	**24**	MOD2	OP	Modulator 2 output.	
33	**25**	VBIAS	OP	Internally generated bias voltage of about $AV_{DD}/2$, except when the device is in 'Powersave' mode when VBIAS will discharge to AV_{SS}. Must be decoupled to AV_{SS} by a capacitor mounted close to the device pins. No other connections allowed.	
34	**26**	MONITOR	OP	Rx Monitor/Rx Eye output	
35	**27**	ADC1	IP	Auxiliary ADC input (1)	Each of the two ADC blocks can select its input signal from any one of these input pins, or from the MIC, ALT or DISC input pins. See section 9.1.3 for details
36	**28**	ADC2	IP	Auxiliary ADC input (2)	
37	**29**	ADC3	IP	Auxiliary ADC input (3)	
38	**30**	ADC4	IP	Auxiliary ADC input (4)	
39	**31**	AVDD	PWR	Positive 3.3V supply rail for the analogue on-chip circuits. Levels and thresholds within the device are proportional to this voltage. This pin should be decoupled to AV_{SS} by capacitors mounted close to the device pins.	
40	**32**	DAC1	OP	Auxiliary DAC output 1/RAMDAC.	
41	**33**	DAC2	OP	Auxiliary DAC output 2.	
42	**34**	AVSS	PWR	Analogue Ground.	
43	**35**	DAC3	OP	Auxiliary DAC output 3.	
44	**36**	DAC4	OP	Auxiliary DAC output 4.	
-	**37**	DVSS	PWR	Digital Ground.	
45	**38**	VDEC	PWR	Internally generated 2.5V supply voltage. Must be decoupled to DV_{SS} by capacitors mounted close to the device pins. No other connections allowed, except for the optional connection to RFV_{DD}.	
46	**39**	XTAL/CLOCK	IP	Input to the oscillator inverter from the Xtal circuit or external clock source.	
47	**40**	XTALN	OP	The output of the on-chip Xtal oscillator inverter.	
48	**41**	DVDD	PWR	The 3.3V positive supply rail for the digital on-chip circuits. This pin should be decoupled to DVss by capacitors mounted close to the device pins.	
49	**42**	CDATA	IP	C-BUS: Serial data input from the µC.	
50	**43**	RDATA	TS OP	C-BUS: A 3-state C-BUS serial data output to the µC. This output is high impedance when not sending data to the µC.	
51	**44**	-	NC	Reserved – do not connect this pin.	

CMX7031 64-pin Q1/L9	CMX7041 48-pin Q3/L4	Signal Name	Type	Description
52	**45**	DVSS	PWR	Digital Ground.
53	-	-	NC	Reserved – do not connect this pin.
54	**46**	SCLK	IP	C-BUS: The C-BUS serial clock input from the µC.
55	**47**	SYSCLK 2	OP	Synthesised Digital System Clock Output 2.
56	**48**	CSN	IP	C-BUS: The C-BUS chip select input from the µC - there is no internal pull-up on this input.
57	-	-	NC	Reserved – do not connect this pin.
58	**1**	EPSI	OP	Serial Memory Serial Interface: SPI bus output.
59	**2**	EPSCLK	OP	Serial Memory Serial Interface: SPI bus clock.
60	**3**	EPSO	IP+PD	Serial Memory Serial Interface: SPI bus input.
61	**4**	EPSCSN	OP	Serial Memory Serial Interface: SPI bus Chip Select.
62	**5**	BOOTEN1	IP+PD	Used in conjunction with BOOTEN2 to determine the operation of the bootstrap program.
63	**6**	BOOTEN2	IP+PD	Used in conjunction with BOOTEN1 to determine the operation of the bootstrap program.
64	**7**	DVSS	PWR	Digital Ground.
EXPOSED METAL PAD	EXPOSED METAL PAD	SUBSTRATE	~	On this device, the central metal pad (which is exposed on Q1 and Q3 packages only) may be electrically unconnected or, alternatively, may be connected to Analogue Ground (AVss). **No other electrical connection is permitted.**

Notes: IP = Input (+ PU/PD = internal pull-up/pull-down resistor)
OP = Output
BI = Bidirectional
TS OP = 3-state Output
PWR = Power Connection
NC = No Connection - should NOT be connected to any signal.

3.1 Signal Definitions

Table 1 Definition of Power Supply and Reference Voltages

Signal Name	Pins	Usage
AV_{DD}	AVDD	Power supply for analogue circuits.
DV_{DD}	DVDD	Power supply for digital circuits.
RFV_{DD}	RFVDD	Power supply for RF synthesiser circuits.
CPV_{DD}	CPVDD	Power supply for RF charge pump.
V_{DEC}	VDEC	Power supply for core logic, derived from DV_{DD} by on-chip regulator.
V_{BIAS}	VBIAS	Internal analogue reference level, derived from AV_{DD}.
AV_{SS}	AVSS	Ground for all analogue circuits.
DV_{SS}	DVSS	Ground for all digital circuits.
RFV_{SS}	RFVSS	Ground for all RF circuits.

4 External Components

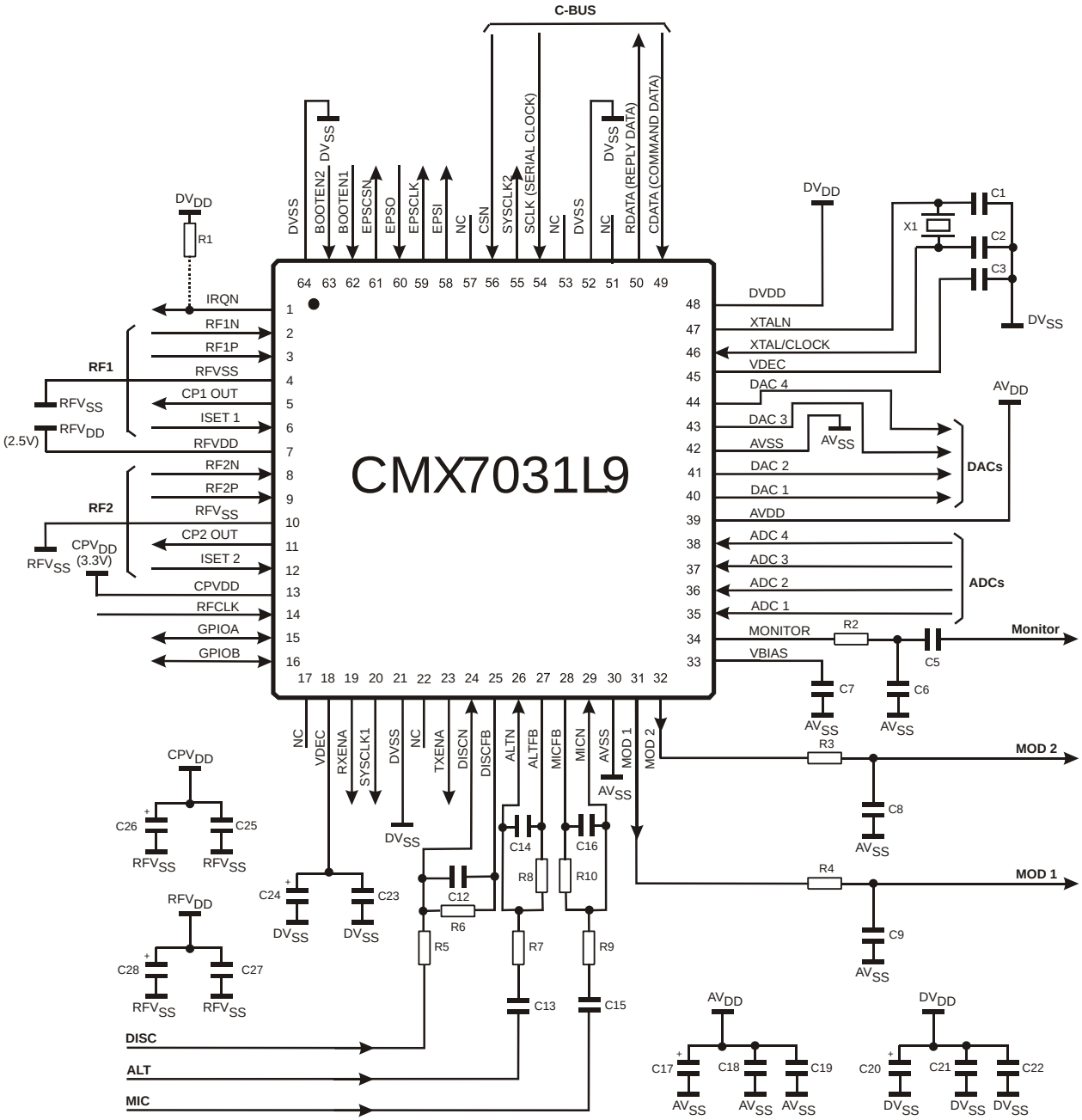


Figure 2 CMX7031 Recommended External Components

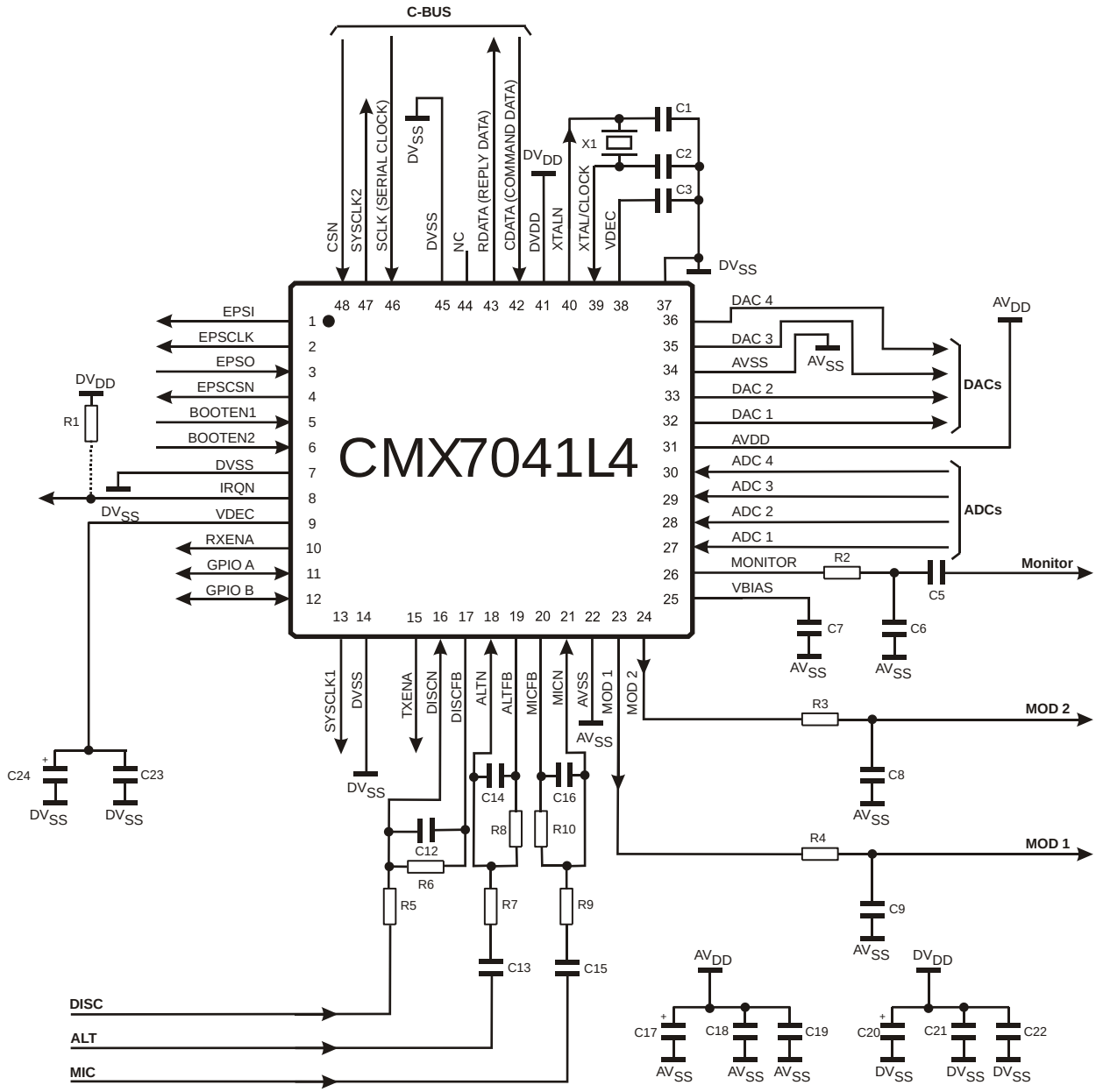


Figure 3 CMX7041 Recommended External Components

R1	100kΩ	C1	18pF	C11	*not used*	C21	10nF
R2	100kΩ	C2	18pF	C12	100pF	C22	10nF
R3	100kΩ	C3	10nF	C13	See note 5	C23	10nF
R4	100kΩ	C4	*not used*	C14	100pF	C24	10µF
R5	See note 2	C5	1nF	C15	See note 5	C25	10nF
R6	100kΩ	C6	100pF	C16	180pF	C26	10µF
R7	See note 3	C7	100nF	C17	10µF	C27	10nF
R8	100kΩ	C8	100pF	C18	10nF	C28	10µF
R9	See note 4	C9	100pF	C19	10nF	X1	12.4MHz
R10	100kΩ	C10	*not used*	C20	10µF		See note 1

Resistors ±5%, capacitors and inductors ±20% unless otherwise stated.

Notes:

1. X1 can be a crystal or an external clock generator; this will depend on the application. The tracks between the crystal and the device pins should be as short as possible to achieve maximum stability and best start up performance. By default, a 19.2MHz oscillator is assumed, other values could be used if the various internal clock dividers are set to appropriate values.

2. R5 should be selected to provide the desired dc gain of the discriminator input, as follows:

$$|GAIN_{DISC}| = 100k\Omega / R5$$

   The gain should be such that the resultant output at the DISCFB pin is within the discriminator input signal range specified in 7.12.2.

3. R7 should be selected to provide the desired dc gain (assuming C13 is not present) of the alternative input as follows:

$$|GAIN_{ALT}| = 100k\Omega / R7$$

   The gain should be such that the resultant output at the ALTFB pin is within the alternative input signal range specified in 7.12.

4. R9 should be selected to provide the desired dc gain (assuming C15 is not present) of the microphone input as follows:

$$|GAIN_{MIC}| = 100k\Omega / R9$$

   The gain should be such that the resultant output at the MICFB pin is within the microphone input signal range specified in 7.12.1. For optimum performance with low signal microphones, an additional external gain stage may be required.

5. C13 and C15 should be selected to maintain the lower frequency roll-off of the discriminator inputs as follows:

$$C13 \geq 1.0\mu F \times |GAIN_{ALT}|$$

$$C15 \geq 30nF \times |GAIN_{MIC}|$$

   For 9600bps GMSK operation the DISCN input should be DC coupled.

6. ALTN and ALTFB connections allow the user to have a second discriminator or microphone input. Component connections and values are as for the respective DISC and MIC networks. If this input is not required, the ALT pin should be connected to AVss.

7. C5 (AUDIO/MONITOR out) should be increased to 1.0µF if frequencies below 300Hz need to be used on this pin. Used for test/debug in this Function Image™.

8. A single 10µF electrolytic capacitor may be fitted in place of C4 and C24, providing the two VDEC pins are connected together on the pcb with an adequate width power supply trace.

5 PCB Layout Guidelines and Power Supply Decoupling

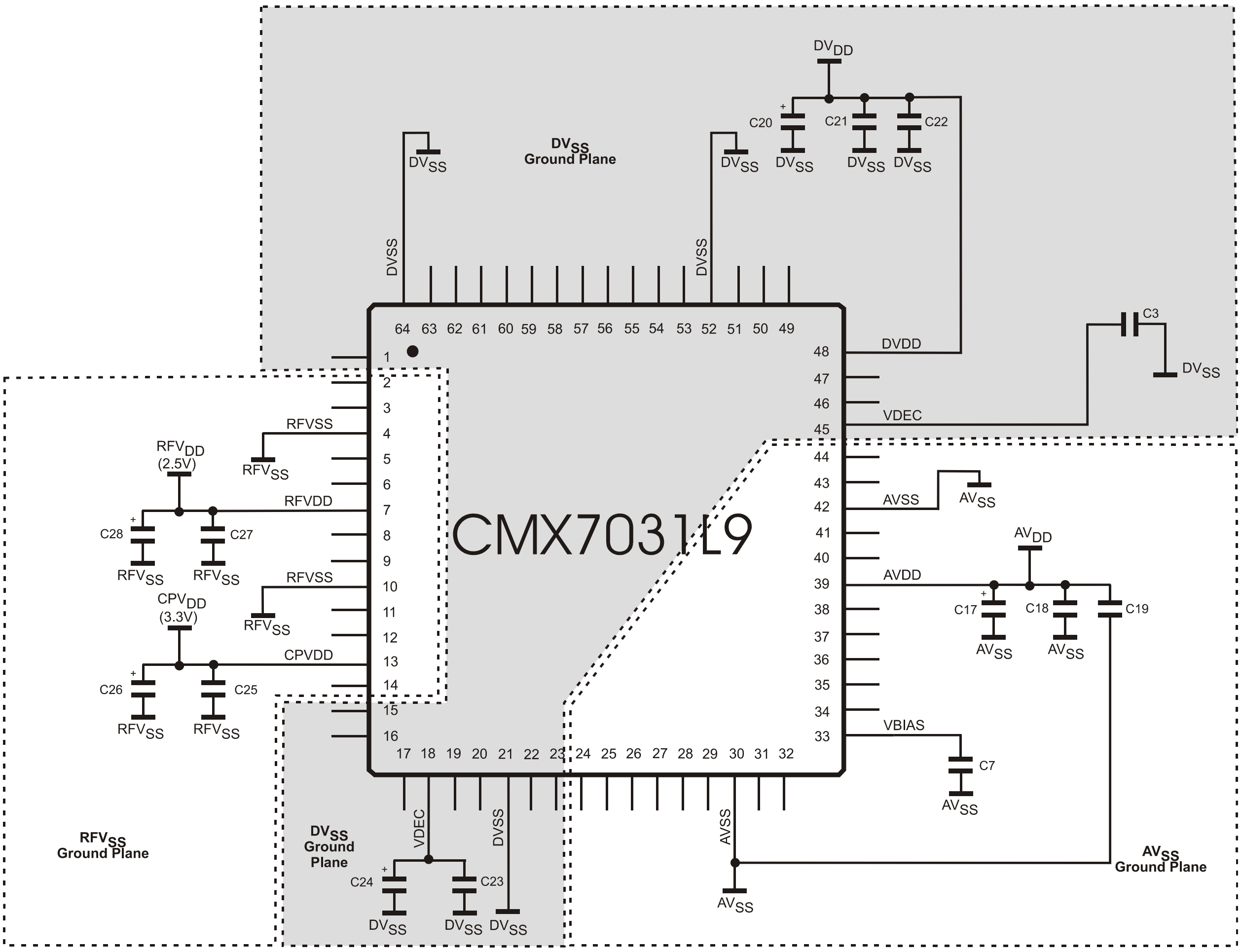


Figure 4 CMX7031 Power Supply Connections and De-coupling

Component Values as per Figure 2.

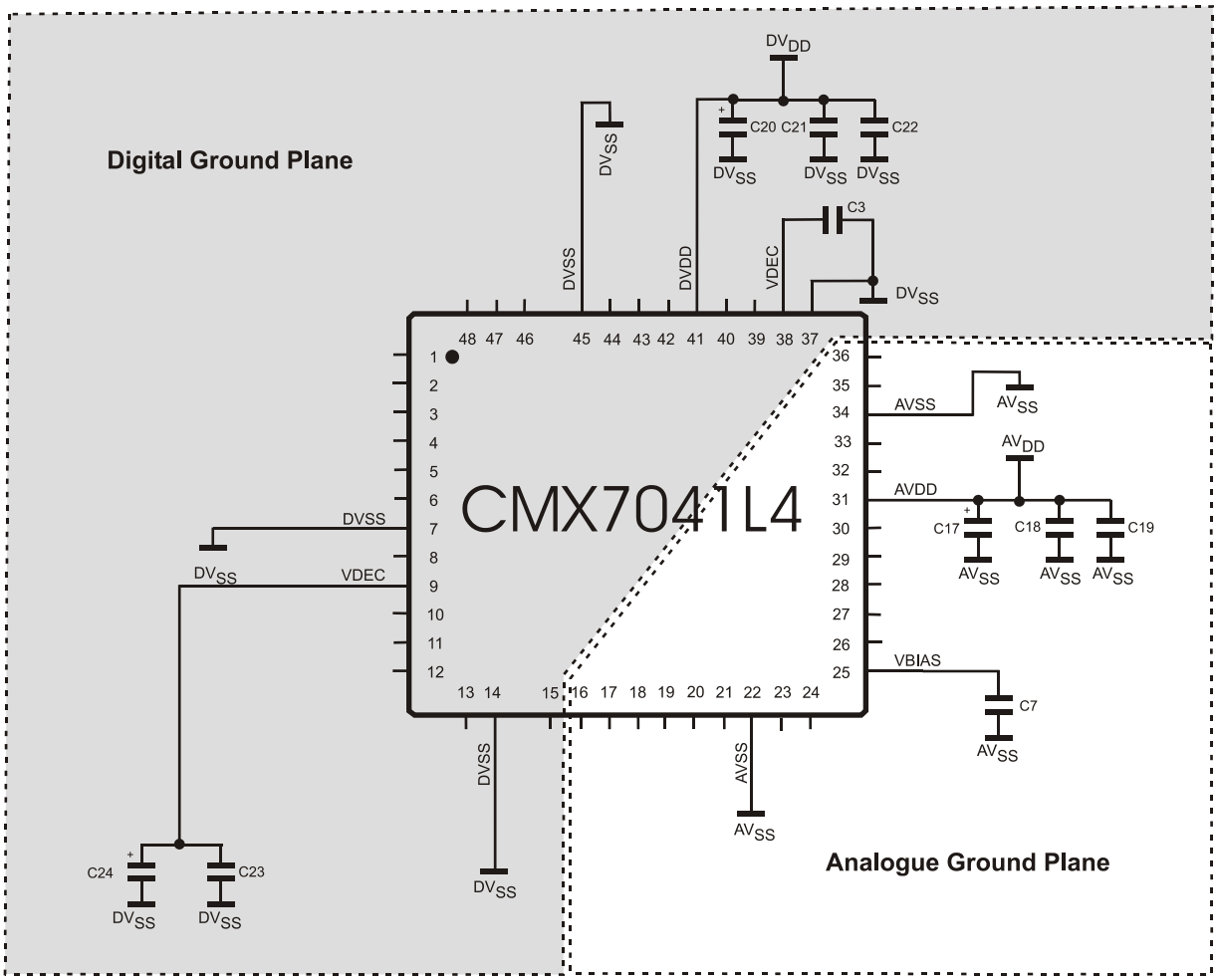


Figure 5 CMX7041 Power Supply Connections and De-coupling

Component Values as per Figure 3.

Notes:

It is important to protect the analogue pins from extraneous inband noise and to minimise the impedance between the device and the supply and bias de-coupling capacitors. The de-coupling capacitors C3, C7, C18, C19, C21, C22, C24 and C25 should be as close as possible to the device. It is therefore recommended that the printed circuit board is laid out with separate ground planes for the AV_{SS}, RFV_{SS} and DV_{SS} supplies in the area of the CMX7031, with provision to make links between them, close to the device. Use of a multi-layer printed circuit board will facilitate the provision of ground planes on separate layers.

V_{BIAS} is used as an internal reference for detecting and generating the various analogue signals. It must be carefully decoupled, to ensure its integrity, so apart from the decoupling capacitor shown, no other loads should be connected. If V_{BIAS} needs to be used to set the discriminator mid-point reference, it must be buffered with a high input impedance buffer.

The crystal X1 may be replaced with an external clock source.

The 2.5V V_{DEC} output can be used to supply the 2.5V RFV_{DD}, to remove the need for an external 2.5V regulated supply. V_{DEC} can be directly connected to RFV_{DD}, in which case C23 should be omitted.

6 General Description

The CMX7031/CMX7041 (7031/7041FI-4.x) are intended for use in half-duplex digital radio equipment and are particularly suited to Amateur Packet Radio using 1200bps or 9600bps data rates and the AX.25 protocol. When both modem speeds are enabled in Rx, the device will automatically decide on which demodulator to activate depending on the reception of a valid sync sequence. For maximal flexibility and compatibility with existing equipment, both modems can detect a $0000007E or $7E7E7E7E sync sequence (32 bits in AFSK and 24 bits in GMSK are required to minimise the effect of "false" detects in the presence of noise). The data is NRZId before being presented to the host over the RxData registers. In Tx mode, the host can decide which mode, 1200bps, 9600bps or DTMF to use. Data is NRZId before transmission. In 9600bps mode the K9NG scrambler is automatically implemented on both Rx and Tx data. Tx Pre-emphasis is included for both 9600bps and 1200bps modes.

A flexible power control facility allows the device to be placed in its optimum powersave mode when not actively processing signals. The CMX7031/CMX7041 include a crystal clock generator, with buffered output, to provide a common system clock if required. A block diagram of the CMX7031/CMX7041 is shown in Figure 1.

The signal processing blocks can be individually routed from any of the three mic/audio/discriminator input pins.

Tx functions:

- Two-point modulation outputs with programmable level adjustment
- Programmable DTMF generator
- 1200bps AFSK modem
- 9600bps GMSK modem
- NRZI encoding
- Tx Pre-emphasis
- K9NG scrambling for 9600bps mode
- Tx Sequencer
- Tx Enable output

Rx functions:

- Demodulator input with input amplifier and programmable gain adjustment
- 1200bps AFSK modem
- 9600bps GMSK modem
- NRZI decoding
- K9NG descrambling for 9600bps mode
- Automatic 1200/9600bps detection
- Multiple sync detection
- Rx Enable output

Auxiliary functions:

- Two flexible Integer-N RF synthesisers (CMX7031 only)
- Two programmable system clock outputs
- Two auxiliary ADCs with selectable input paths
- Four auxiliary DACs, one with built-in programmable RAMDAC

Interface:

- C-BUS, 4-wire, high-speed, synchronous serial command/data bus
- Open drain IRQ to host
- Two GPIO pins
- Serial Memory boot mode
- C-BUS boot mode

7 Detailed Descriptions

7.1 Xtal Frequency

The CMX7031/CMX7041 are designed to work with an external frequency source of 19.2MHz or a 12.4MHz Xtal. At power-on, a 19.2MHz source is selected by default. The 12.4MHz option can be selected by setting the $C3 register appropriately whilst in Idle mode. The correct clock frequency MUST be selected before the device is put into Rx or Tx mode.

7.2 Host Interface

A serial data interface (C-BUS) is used for command, status and data transfers between the CMX7031/CMX7041 and the host µC; this interface is compatible with microwire, SPI. Interrupt signals notify the host µC when a change in status has occurred and the µC should read the status register across the C-BUS and respond accordingly. Interrupts only occur if the appropriate mask bit has been set. See section 7.13.1.

The CMX7031/CMX7041 will monitor the state of the C-BUS registers that the host has written to every 50µs (the C-BUS latency period) hence it is not advisable for the host to make successive writes to the same C-BUS register within this period.

To minimise activity on the C-BUS interface, optimise response times and ensure reliable data transfers, it is advised that the IRQ facility be utilised (using the IRQ mask register, $CE). It is permissible for the host to poll the IRQ pin if the host uC does not support a fully interrupt-driven architecture. This removes the need to continually poll the C-BUS status register ($C6) for status changes.

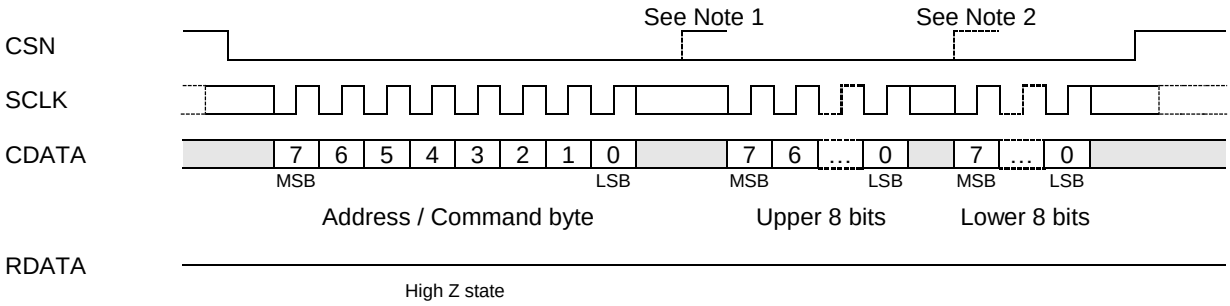
7.2.1 C-BUS Operation

This block provides for the transfer of data and control or status information between the CMX7031/CMX7041's internal registers and the host µC over the C-BUS serial interface. Each transaction consists of a single Address byte sent from the µC which may be followed by one or more Data byte(s) sent from the µC to be written into one of the CMX7031/CMX7041's Write-only registers, or one or more data byte(s) read out from one of the CMX7031/CMX7041's Read-only registers, as illustrated in Figure 6.

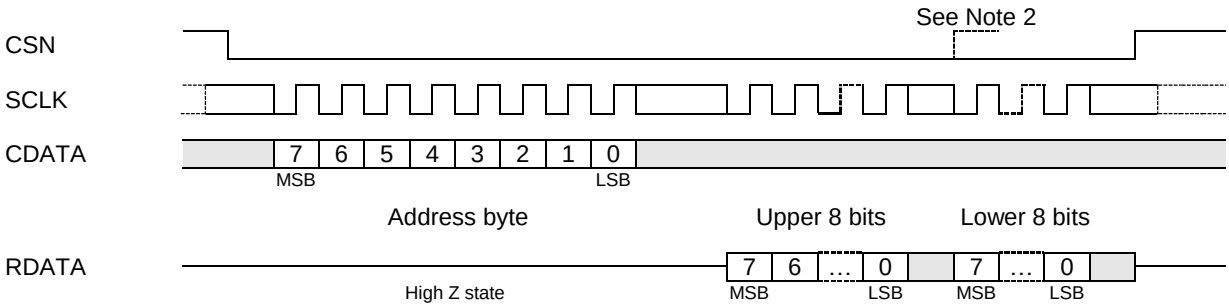
Data sent from the µC on the CDATA line is clocked into the CMX7031/CMX7041 on the rising edge of the SCLK Clock input. RDATA sent from the CMX7031/CMX7041 to the µC is valid when the SCLK is high. The CSN line must be held low during a data transfer and kept high between transfers. The C-BUS interface is compatible with most common µC serial interfaces and may also be easily implemented with general purpose µC I/O pins controlled by a simple software routine.

The number of data bytes following an Address byte is dependent on the value of the Address byte. The most significant bit of the address or data are sent first. For detailed timings see section 8.2. Note that, due to internal timing constraints, there maybe a delay of up to 50µs between the end of a C-BUS write operation and the device reading the data from its internal register. When making multiple writes to the same C-BUS location, ensure that the C-BUS latency period (typically 50µs) is observed.

C-BUS Write:



C-BUS Read:



Data value unimportant

Repeated cycles

Either logic level valid (and may change)

Either logic level valid (but must not change from low to high)

Figure 6 C-BUS Transactions

Notes:

1. For Command byte transfers only the first 8 bits are transferred ($01 = Reset).
2. For single byte data transfers only the first 8 bits of the data are transferred.
3. The CDATA and RDATA lines are never active at the same time. The Address byte determines the data direction for each C-BUS transfer.
4. The SCLK input can be high or low at the start and end of each C-BUS transaction.
5. The gaps shown between each byte on the CDATA and RDATA lines in the above diagram are optional, the host may insert gaps or concatenate the data as required.

7.3 Function Image™ Load and Activation

The Function Image™ (FI) file, which defines the operational capabilities of the device, may be obtained from the CMLTechnical Portal, following product registration. This is in the form of a 'C' header file which can be included into the host controller software or programmed into an external serial memory. The maximum possible size of Function Image™ is 46 kbytes, although a typical FI will be less than this. Note that the BOOTEN pins are only read at power-on or following a C-BUS General Reset and must remain stable throughout the FI loading process. Once the FI load has completed, the BOOTEN pins are ignored by the CMX7031/CMX7041 until the next power-up or C-BUS General Reset.

The BOOTEN pins are both fitted with internal low-current pull-down devices.

For C-BUS load operation, both pins should be pulled high by connecting them to V_{DD} either directly or via a 220kΩ resistor (see Table 2).

For serial memory load, only BOOTEN1 needs to be pulled high in a similar manner, however, if it is required to program the serial memory in-situ from the host, either a jumper to V_{DD} or a link to a host I/O pin should be provided to pull BOOTEN2 high when required (see Table 2).

Once the FI has been loaded, the CMX7031/CMX7041 performs these actions:

1. The product identification code $7031 is reported in C-BUS register $C5
2. The FI version code is reported in C-BUS register $C9
3. The two 32-bit FI checksums are reported in C-BUS register pairs $A9, $AA and $B8, $B9
4. The device waits for the host to load the 32-bit Device Activation Code to C-BUS register $C8
5. once activated, the device initialises fully, enters idle mode and becomes ready for use, and the Programming Flag (bit 0 of the Status register, $C6) will be set.

The checksums should be verified against the published values to ensure that the FI has loaded correctly. Once the FI has been activated, the checksum, product identification and version code registers are cleared and these values are no longer available. If an invalid activation code is loaded, the device will report the value $DEAD in register $A9 and become unresponsive to all further host commands (including General Reset). A power-on reset is required to recover from this state.

The Device Activation Codes are available from the CML Technical Portal. The checksum values are shown in the FI header.

Table 2 BOOTEN Pin States

	BOOTEN2	BOOTEN1
C-BUS Host load	1	1
reserved	1	0
Serial Memory load	0	1
No FI load	0	0

Note: In the rare event that a General Reset needs to be issued without the requirement to re-load the FI, the BOOTEN pins must both be cleared to '0' before issuing the Reset command. The Checksum values will be reported and the Device Activation code will need to be sent in a similar manner as that shown in Figure 8. There will not be any FI loading delay. This assumes that a valid FI has been previously loaded and that V_{DD} has been maintained throughout the reset to preserve the data.

7.3.1 FI Loading from Host Controller

The FI can be included into the host controller software build and downloaded into the CMX7031/CMX7041 at power-up over the C-BUS interface. The BOOTEN pins must be set to the C-BUS load configuration, the CMX7031/CMX7041 powered up and placed into Program Mode, the data can then be sent directly over the C-BUS to the CMX7031/CMX7041.

Each time the device is powered up its Function Image™ must first be loaded and then activated. These two steps assign internal device resources and determine all device features. The device does not operate until the Function Image™ is loaded and activated.

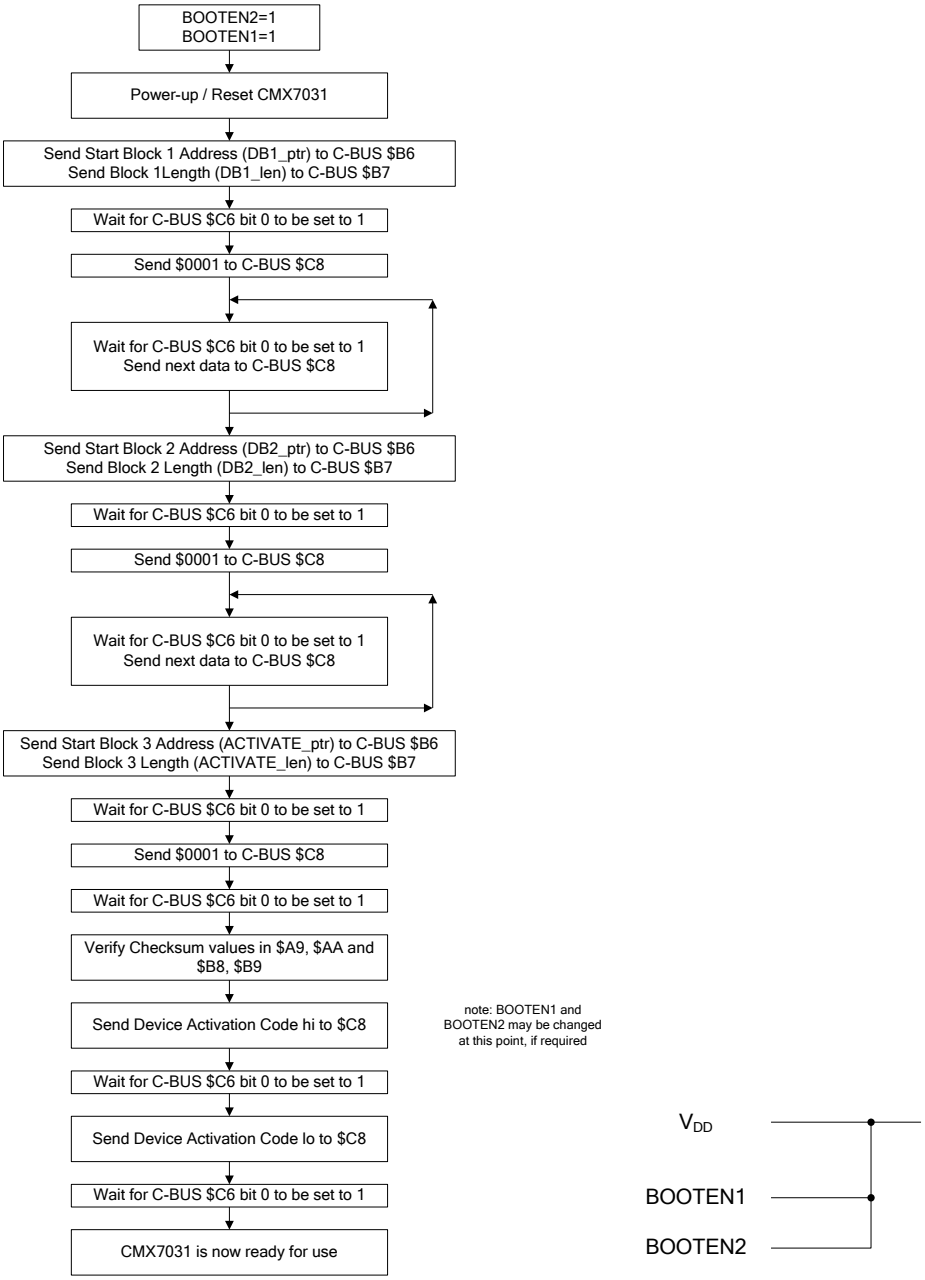


Figure 7 FI Loading from Host

The download time is limited by the clock frequency of the C-BUS, with a 5MHz SCLK, it should take less than 500ms to complete.

7.3.2 FI Loading from Serial Memory

The FI must be converted into a format for the serial memory programmer (normally Intel Hex) and loaded into the serial memory either by the host or an external programmer. The CMX7031/CMX7041 needs to have the BOOTEN pins set to serial memory load, and then on power-on, or following a C-BUS General Reset, the CMX7031/CMX7041 will automatically load the data from the serial memory without intervention from the host controller.

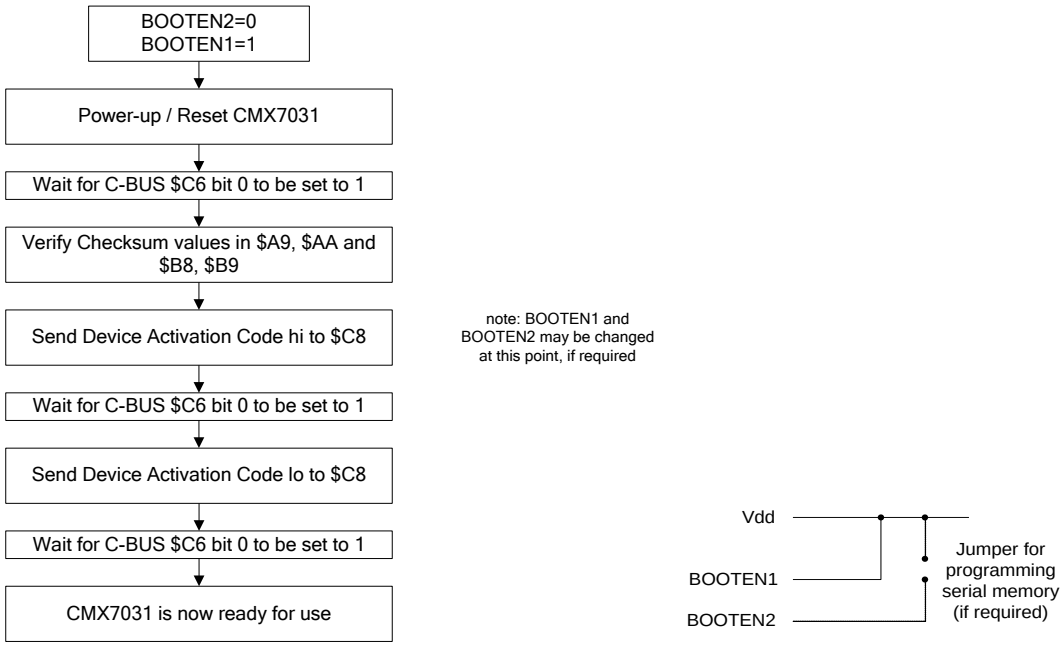


Figure 8 FI Loading from Serial Memory

The CMX7031/CMX7041 has been designed to function with Atmel AT25HP512 serial EEPROM and the AT25F512 flash EEPROM devices[2], however other manufacturers parts may also be suitable. The time taken to load the FI is dependant on the Xtal frequency, with a 6.144MHz Xtal, it should load in less than 1 second.

[2] Note that these two devices have slightly different addressing schemes. FI 4.x is compatible with both schemes.

7.4 Device Control

The CMX7031/CMX7041 should be configured to the mode that suits the environment in which it is to be used. These modes are described in the following sections and are programmed over the C-BUS: either directly to operational registers or, for parameters that are not likely to change during operation, via the Programming register ($C8).

For basic operation:

1. Enable the relevant hardware sections via the Power Down Control register
2. Set the appropriate mode registers to the desired state (Data rate, DTMF Tone etc.)
3. Select the required Signal Routing and Gain
4. Use the Mode Control register to place the device into Rx or Tx mode.

To conserve power when the device is not actively processing an analogue signal, place the device into Idle mode. Additional powersaving can be achieved by disabling the unused hardware blocks, however, care must be taken not to disturb any sections that are automatically controlled.

See:

- Power Down Control - $C0 write
- Mode Control – $C1 write
- Output Level – $C2 write
- Input Gain and Routing - $B1 write

7.4.1 Signal Routing

The CMX7031/CMX7041 offers a flexible routing architecture, with three signal inputs, and a selection of two modulator outputs (to suit two-point modulation schemes). The signal processing blocks can be routed to any of the three input signal pins via Input 1 block. The outputs from signal processing blocks are determined by the settings of the Input Gain And Routing register in Tx mode.

See:

- Input Gain and Routing - $B1 write
- Mode Control – $C1 write

The analogue gain/attenuation of each input and output can be set individually.

See:

- Output Level – $C2 write
- Input Gain and Routing - $B1 write
- GPIO Control - $A7 16-bit write

7.4.2 Mode Control

The CMX7031/CMX7041 operates in one of three modes:

- Idle
- Rx
- Tx

At power-on or following a Reset, the device will automatically enter Idle mode, which allows for the maximum powersaving whilst still retaining the capability of monitoring the AuxADC inputs (if enabled). It is only possible to write to the Programming register whilst in Idle mode.

See:

- Mode Control – $C1 write

7.5 Transmitting DTMF Tones

The DTMF signals to be generated are loaded into b4-0 of the TxData1 register ($B6) from the host whenever the device is in DTMF Tx mode. Setting b5 will generate a “Null” tone. Table 3 shows the DTMF tone pairs,

Table 3 DTMF Tone Pairs

Tone Code (binary)	Tone Code (Hex)	Key Pad Position	Low Tone (Hz)	High Tone (Hz)
00001	01	1	697	1209
00010	02	2	697	1336
00011	03	3	697	1477
00100	04	4	770	1209
00101	05	5	770	1336
00110	06	6	770	1477
00111	07	7	852	1209
01000	08	8	852	1336
01001	09	9	852	1477
01010	0A	0	941	1336
01011	0B	*	941	1209
01100	0C	#	941	1477
01101	0D	A	697	1633
01110	0E	B	770	1633
01111	0F	C	852	1633
00000	00	D	941	1633
1xxxx	1x	null	-	-

7.6 AFSK/GMSK Data Modem

The CMX7031/CMX7041 supports both 1200bps AFSK and 9600bps GMSK data modes. In Rx mode, the device can be set to look for either of the AFSK or GMSK modes, however, once a valid mode has been found, it will stay in that mode until the host resets it.

See:

- Mode Control – $C1 write

7.6.1 Receiving AFSK/GMSK Signals

The CMX7031/CMX7041 can decode incoming AFSK/GMSK signals at either 1200 or 9600 baud data rates, automatically detecting the rate from the received signal. The form of AFSK/GMSK signals for these baud rates is shown in Figure 12.

In 1200bps AFSK mode, the received signal is filtered and data is extracted with the aid of a PLL to recover the clock from the serial data stream. The bit clock is not output externally.

The extracted data is compared with the 32-bit sync pattern which corresponds to either $0000007E or $7E7E7E7E (both are required to ensure compatibility with existing devices already in service) and then NRZI decoded. An interrupt will be flagged when the sync pattern is detected. The host µC may stop the sync search by disabling the AFSK demodulator. Once a valid sync pattern has been detected, the sync search algorithm is disabled; it may be re-started by the host re-writing to the Mode register ($C1:b4,5) with the modem and mode bits set appropriately. The recovered data is NRZI decoded and is held in an 256-byte internal buffer, from where it can be read by the host over C-BUS using the RxData block. A DataRDY flag will be raised whenever there is data available in the buffer. Data is transferred over the C-BUS under host µC control. The host should ensure that the data is transferred at an adequate rate following data ready being flagged.

The host µC must keep track of the message length, or otherwise determine the end of reception, and disable the demodulator at the appropriate time.

In 9600bps GMSK mode, the received signal is fed through a Gaussian filter with a Bt of 0.5. The device extracts timing and level information from the 24-bit sync pattern. Once a valid sync pattern has been detected, the extracted data is de-scrambled and NRZI decoded in a similar manner to the 1200bps mode.

Note that once a particular mode (1200 or 9600) signal has been detected, the other demodulator is switched off. Hence, after a data burst has been received by the host it should re-set both Modem Control bits of the Mode register ($C1:b2,3) and then re-enable them (taking note of the C-BUS latency time).

In both GMSK and AFSK modes, a single bit error is allowed during the sync sequence detection.

7.6.2 Transmitting AFSK/GMSK Data

The CMX7031/CMX7041 will transmit all data transferred from the host over C-BUS at either 1200 or 9600bps as selected by the Mode Control register ($C1: b4,5).

The binary over-air data is taken from the device's internal buffer which is loaded from the host using the TxData register block, most significant bit first. The data must be provided over the C-BUS from the host within certain time limits to ensure the selected baud rate is maintained and an underflow condition does not occur. The device's internal buffer is 256 bytes long and may be pre-loaded by the host before the Tx Modulator is enabled. The host must supply ALL data to be transmitted, including any preamble that may be required during the TxDelay period that precedes the actual data packet. The TxDataRDY flag will be raised whenever there is room for a host to write a full TxData block. The TxDataRDY flag will be inhibited when there are less than 4 bytes left empty in the buffer.

A Tx sequencer state machine is provided to automate the transmission of data bursts. The timings of the sequencer can be pre-programmed by the host to suit the characteristics of the radio hardware. The sequencer controls:

Table 4 TxSequencer Timing

	ticks	ms	ms (cumulative)
TxENA active	0	0	0
Ramp Up Start Delay	240	10	10
Modulation Start Delay	240	20	30

…data will now be transmitted from the TxData block via the TxData buffer until the "Last Data" flag is asserted by the host.

Ramp Down Start Delay	240	10	10
TxENA Inactive	240	10	20

All sequencer timing values are specified in terms of 24kHz "ticks". Default values are shown in the tables.

The Modulation Start Delay allows for a period of un-modulated carrier to be output at the beginning of the burst. The value chosen for this item should also take into account the time it takes for the RAMDAC to complete its cycle (default is 10ms).

The Ramp Down Start Delay allows for a period of un-modulated carrier at the end of the burst if required.

The TxENA Inactive delay value chosen for this item should also take into account the time it takes for the RAMDAC to complete its cycle (default is 10ms). Note that Program Register P3.0:b0 should be set to enable RAMDAC operation.

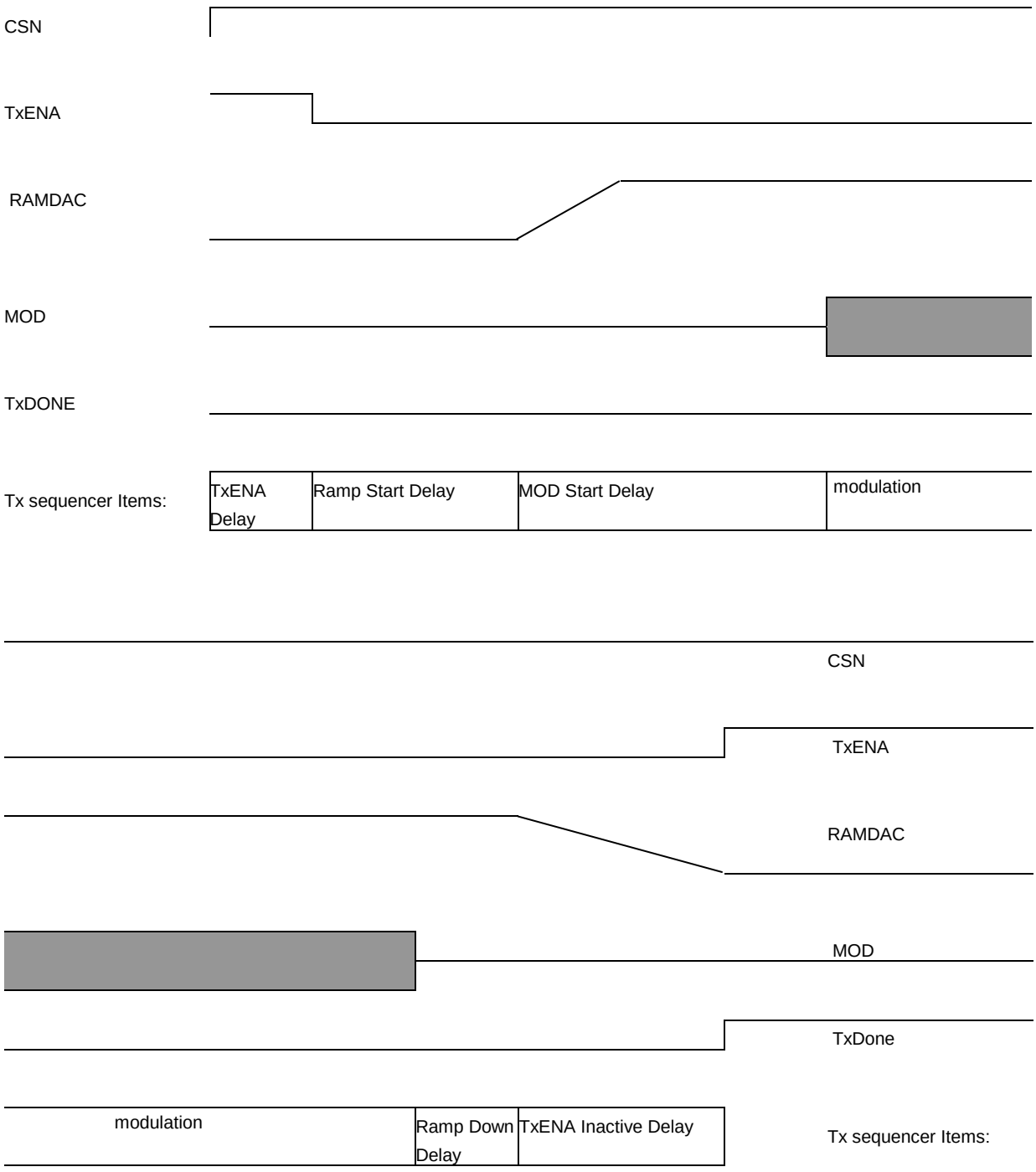


Figure 9 Ramp-up and Ramp-down Sequences

Typical stages of Tx operation are depicted in Figure 10 and occur as follows:

1. The host writes up to four words of data for transmission into the TxData C-BUS registers.
2. The host writes to the TxData Count register, specifying the number of bytes/bits to transfer This results in the transfer of the data from the TxData registers into the Tx Data Buffer.
3. Steps 1 and 2 can be repeated to load the Tx Data Buffer with a large block of data.
4. The Mode bits are set to Tx, which causes the Tx sequencer to activate and data to be NRZId (and scrambled in the case of 9600bps mode) and passed to the Tx Modulator and transmitted to the MOD1 and MOD2 output pins.
5. This will continue until such time that the host notifies the device by setting the “Last Data” bit in the TxData Count register, at which point the Modulator will cease operation once the last data bit has been transmitted. At this point the Tx sequencer will de-activate and the TxENA line will return to its inactive state and assert the TxDone IRQ when the host may turn off any other directly controlled Tx circuits/processes. The sequencer automatically compensates for data transfer and internal processing/filtering delays.
6. If the host does not supply sufficient data, a data famine condition will be indicated and the Tx sequencer will execute as if the “Last Data” flag had been asserted.

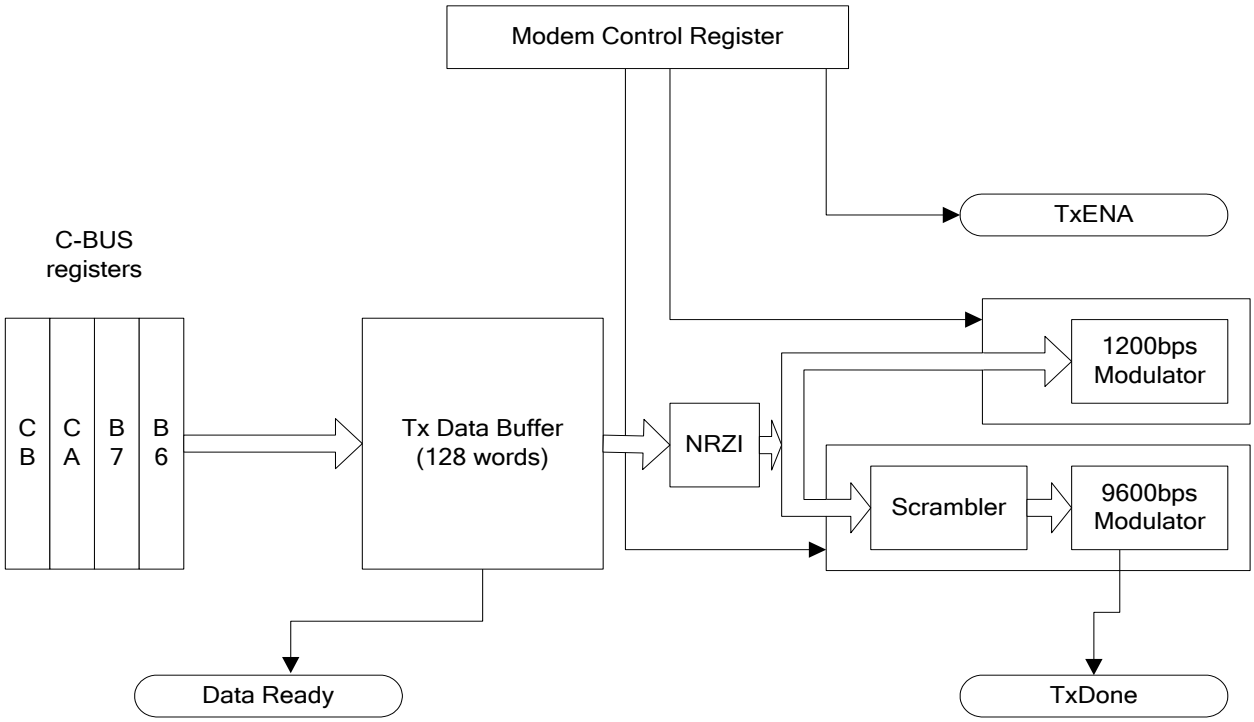


Figure 10 Tx Operation

7.6.3 Receiving AFSK/GMSK Data

When enabled and subsequent to the sync sequence being detected, the selected demodulator will NRZI the data and deliver data bits to the internal Rx buffer. This data is transferred to the C-BUS RxData block and the RxDataRDY IRQ activated.

Typical stages of Rx operation are depicted in Figure 11 and occur as follows:

1. The host detects the Sync detect IRQ becoming active, at which point the device will start to transfer received data bits to the internal buffer and transfer the first four words of data to the C-BUS RxData registers
2. The host detects the RxDataRDY IRQ becoming active
3. The host reads 4 words from the RxData C-BUS registers
4. Steps 2 and 3 can be repeated until the host detects the end of the data burst
5. The host writes to the Mode Control register to either:
    a. Disable Rx mode, at which point RxENA will become inactive and the demodulator, NRZI, synch detect blocks will become inactive
    b. Write to the Mode Control register with the mode bits set for Rx, which will cause the modem to re-start its sync detect process

Note that the demodulator will continue to deliver data until the host shuts it down, even if the signal at the input is no longer valid.

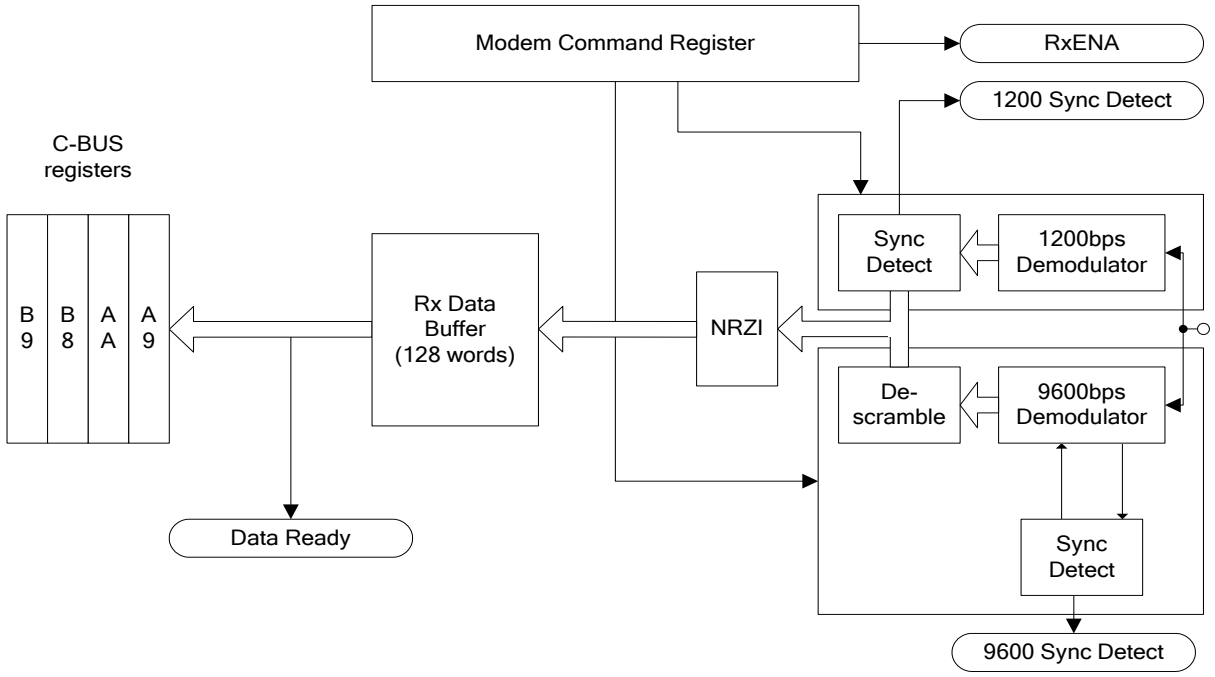


Figure 11 Rx Operation

7.6.4 1200bps AFSK Modem

The 1200bps AFSK encoding operates in accordance with the bit settings in the Modem Command register ($C1). NRZI encoding is applied to all transmitted bits.

The CMX7031/CMX7041FI-4.x generates its own internal data clock and converts the binary data into the appropriately phased frequencies, as shown in Figure 12 and Table 5.

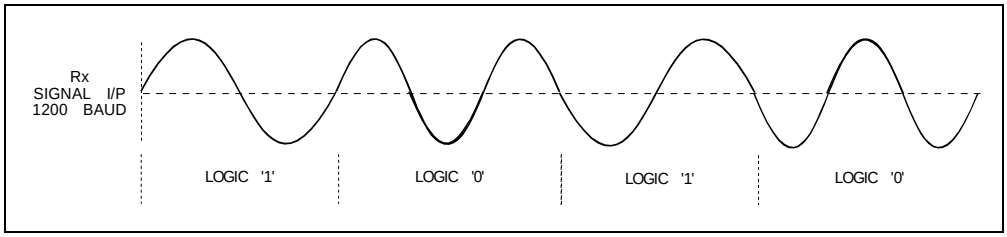


Figure 12 Modulating Waveform for 1200bps AFSK Signals

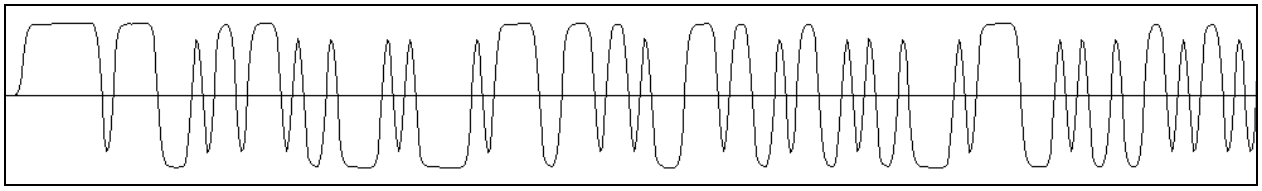


Figure 13 Modulating Waveform for 9600bps GMSK Signals

Table 5 Data Frequencies for 1200bps

Baud Rate	Data	Frequency
1200baud	1	1200Hz
	0	2200Hz

In receive mode, a PLL is used to extract the data from the incoming signal.

7.6.5 9600bps GMSK Modem

The 9600bps GMSK modem directly modulates the RF carrier via the MOD1 and MOD2 signals (two point modulation). The data stream from the host is first filtered via a Gaussian filter with a Bt of 0.5 in order to maximise the signal for efficient reception but at the same time meet the channel emission mask so as not to interfere with adjacent channel users. If the modulator is capable of being dc coupled, then single point modulation can be employed, otherwise it is necessary to modulate both the VCO and the Reference of the Tx PLL to maintain the required frequency response and modulation fidelity.

In addition to the NRZI encoding used in 1200bps operation, the GMSK signal is also passed through a data scrambler to reduce the dc content of the transmitted signal. This is based on a 17-bit maximum length LFSR scrambler.

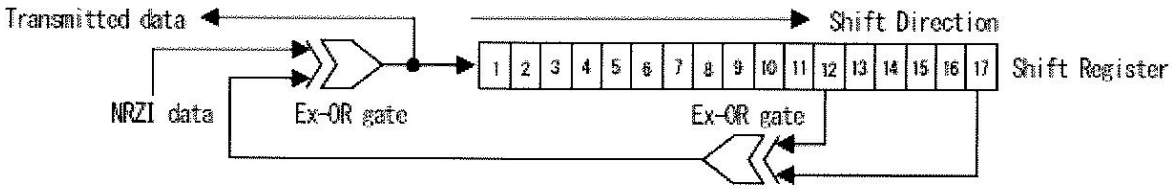


Figure 14 9600bps Data Scrambler

7.7 Auxiliary ADC Operation

The inputs to the two auxiliary ADCs can be independently routed to any of the Signal Input pins under control of the AuxADC, $A7. Conversions will be performed as long as a valid input source is selected, to stop the ADCs, the input source should be set to “none”. Register $C0, b6, BIAS, must be enabled for Auxiliary ADC operation.

Averaging can be applied to the ADC readings by selecting the b2-0 in the Program Block P1.2 and P1.3. This is a rolling average system such that a proportion of the current data value will be added to the last value. The proportion is determined by the value of the average counter.

Table 6 Averaging Values

P1.2/P1.3:b2-0		% of current sample value used	% of previous average used
000	0	100%	0%
001	1	50%	50%
010	2	25%	75%
011	3	12.5%	87.5%
100	4	6.25%	93.75%
101	5	3.125%	96.875%

High thresholds may be independently applied to both ADC channels (the comparison is applied after averaging, if this is enabled) and an IRQ generated if a rising edge passes the high threshold. This feature can be used to as a "Carrier Detect" function when the input is connected to a suitable RF level measurement point in the RF hardware. The thresholds are programmed via the Program Block, P1.0 and P1.1.

Auxiliary ADC data is read back in the AuxADC Data registers ($A9 and $AA) and includes the threshold status as well as the actual conversion data (subject to averaging, if enabled).

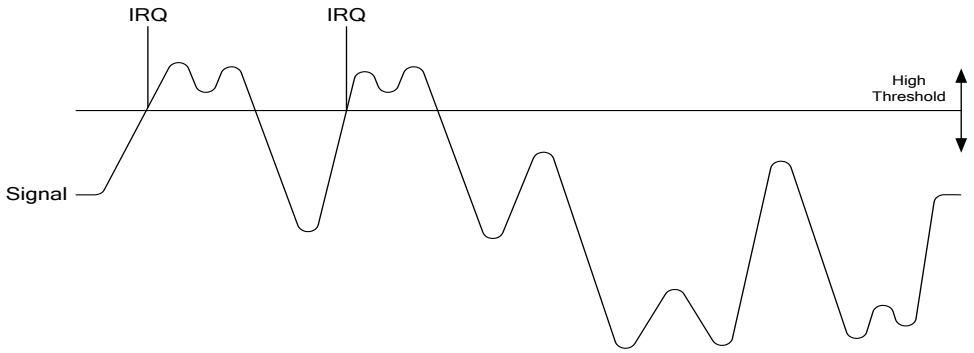


Figure 15 AuxADC IRQ Operation

See:

- AuxADC1 Data - $A9 16-bit read
- AuxADC2 Data - $AA 16-bit read

7.8 Auxiliary DAC/RAMDAC Operation

The four auxiliary DAC channels are programmed via the AuxDAC Control register, $A8. AuxDAC channel 1 may also be programmed to operate as a RAMDAC which will automatically output a pre-programmed profile at a programmed rate.

The default profile is a raised cosine (see Table 11), but this may be over-written with a user defined profile by writing to Programming Block P3.11. The RAMDAC operation is only available in Tx mode and, to avoid glitches in the ramp profile, it is important not to change to IDLE or Rx mode whilst the RAMDAC is still ramping. The AuxDAC outputs hold the user-programmed level during a powersave operation if left enabled, otherwise they will become tri-state (high impedance). Note that access to all four AuxDACs is controlled by the AuxDAC Control register, $A8, and therefore to update all AuxDACs requires four writes to this register. It is not possible to simultaneously update all four AuxDACs.

See:
- AuxDAC Control - $A8 16-bit write

7.9 RF Synthesiser (CMX7031 only)

The CMX7031 includes two Integer-N RF synthesisers, each comprising a divider, phase comparator and charge pump. The divider has two sets of N and R registers: one set can be used for transmit and the other for receive. The division ratios can be set up in advance by means of C-BUS registers. A single C-BUS command will change over from the transmit to the receive division ratios, or vice versa, enabling a fast turnaround.

See:
- RF Channel Data - $B2 write
- RF Channel Control - $B3 write
- RF Channel Status - $B4 8-bit read

External RF components are needed to complete the synthesiser circuit. A typical schematic for one synthesiser, with external components, is shown in Figure 16.

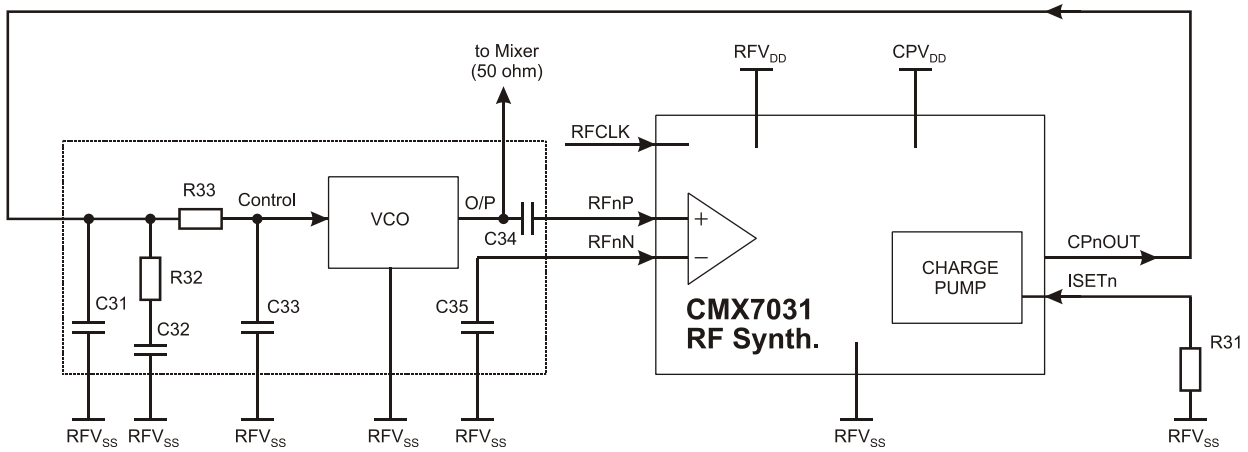


Figure 16 Example RF Synthesiser Components for a 512MHz Receiver

R31	0Ω	C31	820pF
R32	18kΩ	C32	8.2nF
R33	18kΩ	C33	680pF
		C34	1nF
		C35	1nF

Resistors ±5%, capacitors and inductors ±20% unless otherwise stated.

Notes: R31 is chosen within the range 0Ω to 30kΩ and selects the nominal charge pump current.

It is recommended that C34 and C35 are kept close to the VCO and that the stub from the VCO to the CMX7031 is kept as short as possible. The loop filter components should be placed close to the VCO.

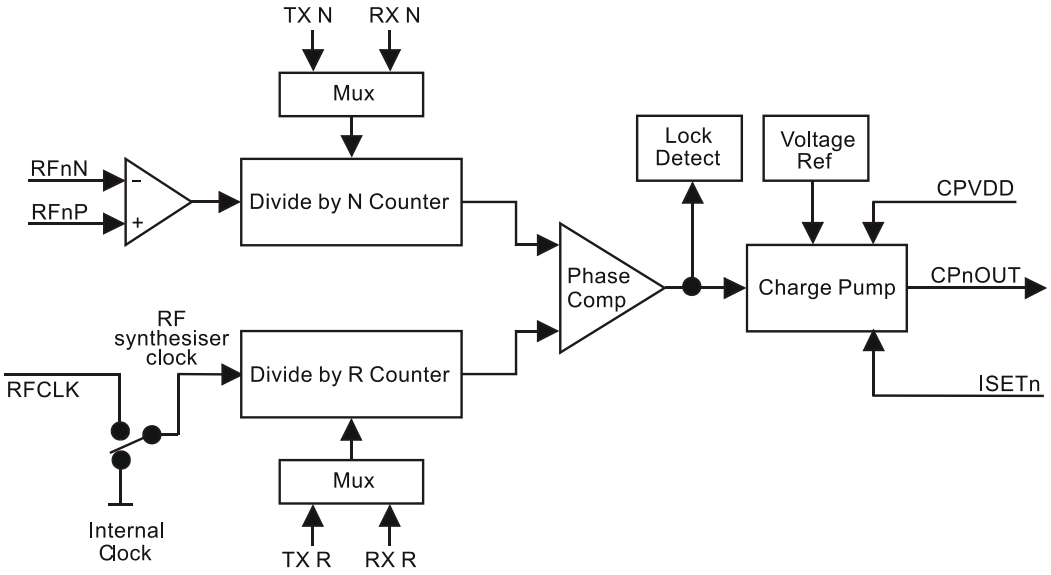


Figure 17 Single RF Channel Block Diagram

The two RF synthesisers are programmable to any frequency in the range 100MHz to 600MHz. Figure 17 is a block diagram of one synthesiser channel. The RF synthesiser clock is selectable between the Xtal or the clock supplied to the RFCLK input pin. The RF synthesiser clock is common to both channels. The charge pump supply (CP supply, CPV_{DD}) is also common to both channels. The +/-RF in pins, Cpout, Iset and RFVSS pins are channel specific and designated as either RF1N, RF1N, CP1OUT, ISET1, RFVSS or RF2P, RF2N, CP2OUT, ISET2, RFVSS on the Signal List in section 3. The N and R values for Tx and Rx modes are channel specific and can be set from the host µC via the C-BUS. Various channel specific status signals are also accessible via C-BUS. The divide by N counter is 20 bits; the R counter is 13 bits. Typical external components are shown in Figure 16.

Both synthesisers are phase locked loops (PLLs) of the same design, utilising external VCOs and loop filters. The VCOs need to have good phase noise performance although it is likely that the high division ratios used will result in the dominant noise source being the reference oscillator. The phase detectors are of the phase-frequency type with a high impedance charge pump output requiring just passive components in the loop filter. Lock detect functions are built in to each synthesiser and the status reported via C-BUS. A transition to out-of-lock can be detected and communicated via a C-BUS interrupt to the host µC. This can be important in ensuring that the transmitter cannot transmit in the event of a fault condition arising.

Two levels of charge pump gain are available to the user, to facilitate the possibility of locking at different rates under program control. A current setting resistor (R31) is connected between the ISET pin (one for each PLL system) and the respective RFV_{SS}. This resistor will have an internally generated band gap voltage expressed across it and may have a value of 0Ω to 30kΩ, which (in conjunction with the on-chip series resistor of 9.6kΩ) will give charge pump current settings over a range of 2.5mA down to 230µA (including the control bit variation of 4 to 1). The value of the current setting resistor (R31) is determined in accordance with the following formulae:

Gain bit set to 1: R31 (in Ω) = (24/Icp) – 9600
Gain bit cleared to 0: R31 (in Ω) = (6/Icp) – 9600

where Icp is the charge pump current (in mA).

Note that the charge pump current should always be set to at least 230µA. The ‘gain bit’ refers to either bit 3 or bit 11 in the RF Channel Control register, $B3.

The step size (comparison frequency) is programmable; to minimise the effects of phase noise this should be kept as high as possible. This can be set as low as 2.5kHz (for a reference input of 20MHz or less), or up to 200kHz – limited only by the performance of the phase comparator.

The frequency for each synthesiser is set by using two registers: an 'R' register that sets the division value of the input reference frequency to the comparison frequency (step size), and an 'N' register that sets the division of the required synthesised frequency from the external VCO to the comparison frequency. This yields the required synthesised frequency (Fs), such that:

$$Fs = (N / R) \times F_{REF}$$ where F_{REF} is the selected reference frequency

Other parameters for the synthesisers are the charge pump setting (high or low):

- Since the set-up for the PLLs takes 4 x "RF Channel Data register" writes it follows that, while updating the PLL settings, the registers may contain unwanted or intermediate values of bits. These will persist until the last register is written. It is intended that users should change the content of the "RF Channel Data register" on a PLL that is disabled, powersaved or selected to work from the alternate register set ("Tx" and "Rx" are alternate register sets). There are no interlocks to enforce this intention. The names "Tx" and "Rx" are arbitrary and may be assigned to other functions as required. They are independent sets of registers, one of which is selected to command each PLL by changing the settings in the RF Channel Control - $B3 write register.

For optimum performance, a common master clock should be used for the RF synthesisers (RF Clock) and the baseband sections (Main and Auxiliary System Clocks). Using unsynchronised clocks can result in spurious products being generated in the synthesiser output and in some cases difficulty may be experienced with obtaining lock in the RF synthesisers.

Lock Status

The lock status can be observed by reading the RF Channel Status register, $B4, and the individual lock status bits can (subject to masking) provide a C-BUS interrupt.

The lock detector can use a tolerance of one cycle or four cycles of the reference clock (not the divided version that is used as a comparison frequency) in order to judge phase lock. An internal shift register holds the last three lock status measurements and the lock status bits are flagged according to a majority vote of these previous three states. Hence, one occasional lock error will not flag a lock fail. At least two successive phase lock events are required for the lock status to be true. Note that the lock status bits confirm phase lock to the measured tolerance and not frequency lock. The synthesiser may take more time to confirm phase lock with the lock status bits than the time to switch from channel to channel. The purpose of a 4-cycle tolerance is for the case where a high frequency reference oscillator would not forgive a small phase error.

RF Inputs

The RF inputs are differential and self biased (when not powersaved). They are intended to be capacitatively coupled to the RF signal. The signal should be in the range 0dBm to –20dBm (not necessarily balanced). To ensure an accurate input signal the RF should be terminated with 50Ω as close to the chip as possible and with the "+" and "–" inputs capacitatively coupled to the input and ground, keeping these connections as short as possible. The RF input impedance is almost purely capacitative and is dominated by package and printed circuit board parasitics.

Guidelines for using the RF Synthesisers

- RF input slew rate (dv/dt) should be 14 V/µs minimum.
- The RF Synthesiser 2.5V digital supply can be powered from the VDEC output pin.
- RF clock sources and other, different clock sources must not share common IC components, as this may introduce coupling into the RF. Unused ac-coupled clock buffer circuits should be tied off to a dc supply, to prevent them oscillating.
- It is recommended that the RF Synthesisers are operated with maximum gain Iset (ie. Iset tied to RFVss).
- The loop filter components should be optimised for each VCO.

7.10 Digital System Clock Generators

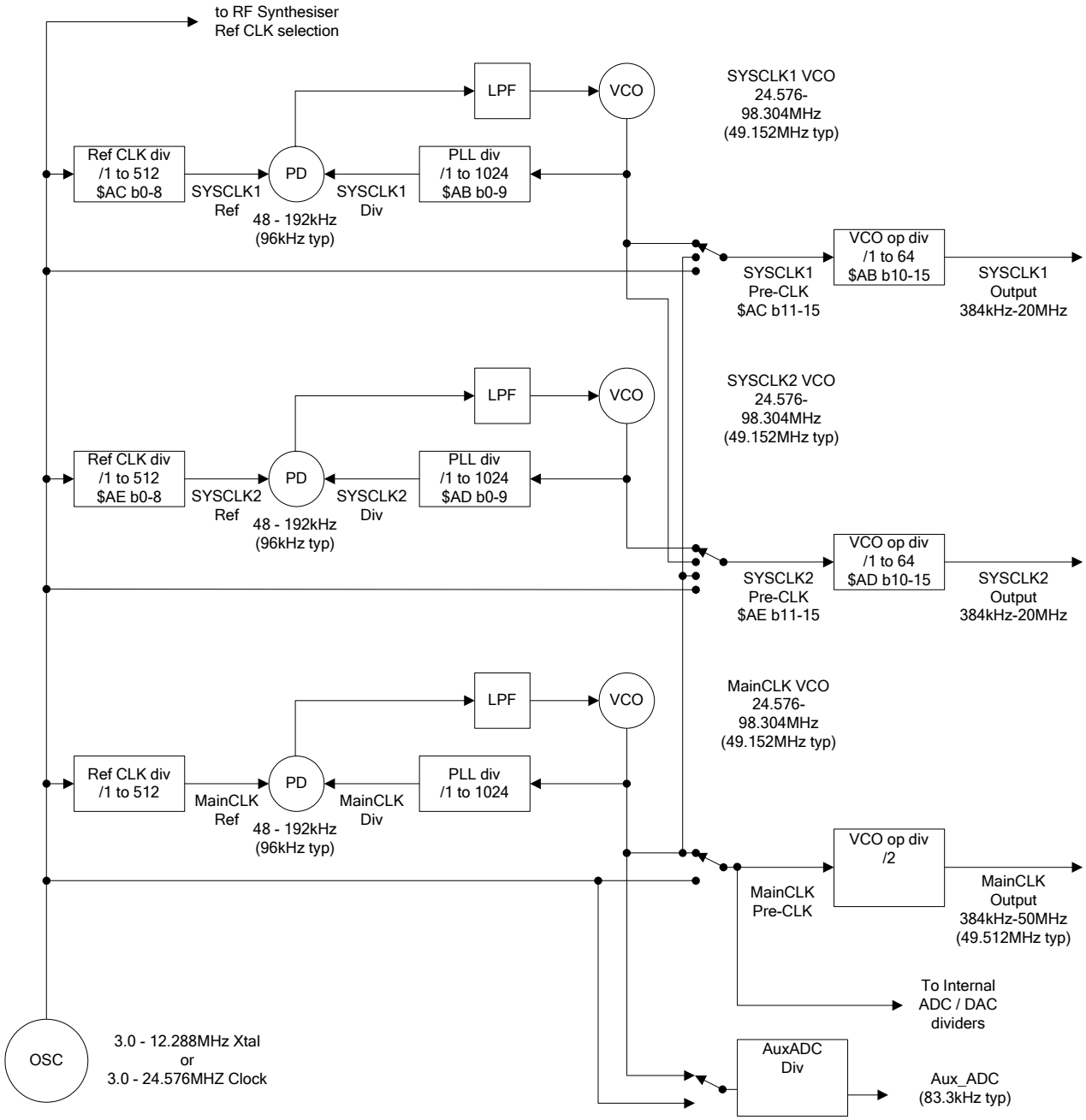


Figure 18 Digital Clock Generation Schemes

The CMX7031/CMX7041 includes a two-pin crystal oscillator circuit. This can either be configured as an oscillator, as shown in section 5, or the XTAL input can be driven by an externally generated clock. The crystal (Xtal) source frequency can go up to 12.288MHz (clock source frequency up to 24.576MHz), but a 19.2MHz oscillator is assumed for the functionality provided in the CMX7031/CMX7041.

7.10.1 Main Clock Operation

A PLL is used to create the Main Clock (nominally 49.512MHz) for the internal sections of the CMX7031/CMX7041. At the same time, other internal clocks are generated by division of either the XTAL Reference Clock or the Main Clock. These internal clocks are used for determining the sample rates and conversion times of A-to-D and D-to-A converters, running a General Purpose Timer, the signal processing block and the RF Synthesisers.

The CMX7031/CMX7041 defaults to the settings appropriate for a 19.2Hz oscillator, with 12.4MHz selection available by setting $C3 appropriately.

See:

- Clock Control - $C3 write

7.10.2 System Clock Operation

Two System Clock outputs, SYSCLK1 and SYSCLK2, are available to drive additional circuits, as required. These are phase locked loop (PLL) clocks that can be programmed via the System Clock registers with suitable values chosen by the user. The System Clock PLL Configure registers ($AB and $AD) control the values of the VCO Output divider and Main Divide registers, while the System Clock Ref. Configure registers ($AC and $AE) control the values of the Reference Divider and signal routing configurations. The PLLs are designed for a reference frequency of 96kHz. If not required, these clocks can be independently powersaved. The clock generation scheme is shown in the block diagram of Figure 18. Note that at power-on, these pins provide, by default:

CMX7031: XTAL clk
CMX7041: no signal (off)

See:

- SYSCLK 1 and 2 PLL data - $AB, $AD write
- SYSCLK1 and 2 REF - $AC and $AE write

7.11 GPIO

Four pins on the device are provided for GPIO purposes. GPIO 1 and 2 are driven by the CMX7031/CMX7041 to follow the state of the Rx and Tx Mode bits in the Mode register, $C1:

Table 7 GPIO States

$C1 Mode	b1	b0	TxENA	RxENA
Idle	0	0	1	1
Rx	0	1	1	0
Tx	1	0	0	1
reserved	1	1	1	1

The timing of the TxENA signal is defined by the Tx Sequencer values. At power-on, their default state is high impedance input. GPIO A and B may be driven or read under host control.

See:

- GPIO Control - $A7 16-bit write

7.12 Signal Level Optimisation

The internal signal processing of the CMX7031/CMX7041 will operate with wide dynamic range and low distortion only if the signal level at all stages in the signal processing chain is kept within the recommended limits. For a device working from a 3.3V ±10% supply, the maximum signal level which can be accommodated without distortion is [(3.3 x 90%) – (2 x 0.3V)] Volts pk-pk = 838mV rms, assuming a sine wave signal. Compared to the reference level of 308mV rms, this is a signal of +8.69dB. This should not be exceeded at any stage. The various level adjustment facilities are shown in Figure 19.

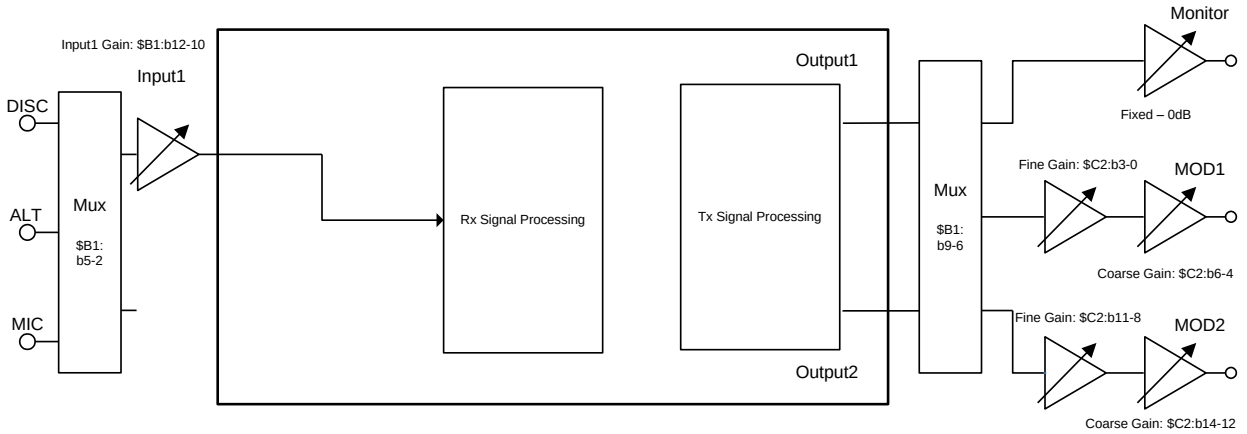


Figure 19 Level Adjustments

7.12.1 Transmit Path Levels

For the maximum signal out of the MOD1 and MOD2 attenuators, the signal level at the output of the Analogue Routing block should not exceed +8.69dB, assuming both fine and coarse output attenuators are set to a gain of 0dB.

7.12.2 Receive Path Levels

The Input Gain adjustment has a variable gain of up to +22.4dB and no attenuation. If the highest gain setting were used, then the maximum allowable input signal level at the DISCFB pin would be 12.0mV rms. With the lowest gain setting (0dB), the maximum allowable input signal level at the DISCFB pin would be +8.69dB (838mVrms) which is an absolute maximum, which should not be exceeded anywhere in the signal processing chain if severe distortion is to be avoided.

7.13 C-BUS Register Summary

Table 8 C-BUS Registers

ADDR. (hex)		REGISTER	Word Size (bits)
$01	W	C-BUS RESET	0
$A7	W	GPIO Control - $A7 16-bit write	16
$A8	W	AuxDAC Control - $A8 16-bit write	16
$A9	R	AuxADC1 Data - $A9 16-bit read/Checksum 2 hi	16
$AA	R	AuxADC2 Data - $AA 16-bit read/Checksum 2 lo	16
$AB	W	SYSCLK1 PLL Data	16
$AC	W	SYSCLK1 Ref	16
$AD	W	SYSCLK2 PLL Data	16
$AE	W	SYSCLK2 Ref	16
$AF		*reserved*	
$B0		*reserved*	
$B1	W	Input Gain and Routing - $B1 write	16
$B2	W	RF Channel Data	16
$B3	W	RF Channel Control	16
$B4	R	RF Channel Status	8
$B5	W	TxData Count - $B5 write	16
$B6	W	TxData Write Block - $B6, $B7, $CA, $CB write	16
$B7	W	TxData Write Block - $B6, $B7, $CA, $CB write	16
$B8	R	RxData Read Block - $B8, $B9, $BA, $BB read/Checksum 1 hi	16
$B9	R	RxData Read Block - $B8, $B9, $BA, $BB read/Checksum 1 lo	16
$BA	R	RxData Read Block - $B8, $B9, $BA, $BB read	16
$BB	R	RxData Read Block - $B8, $B9, $BA, $BB read	16
$BC		*reserved*	
$BD		*reserved*	
$BE		*reserved*	
$BF		*reserved*	
$C0	W	Power Down Control - $C0 write	16
$C1	W	Mode Control – $C1 write	16
$C2	W	Output Level – $C2 write	16
$C3	W	Clock Control - $C3 write	16
$C4		*reserved*	
$C5		*reserved*	
$C6	R	Status – $C6 read	16
$C7		*reserved*	
$C8	W	Programming Register – $C8 write	16
$C9		*reserved*	
$CA	W	TxData Write Block - $B6, $B7, $CA, $CB write	16
$CB	W	TxData Write Block - $B6, $B7, $CA, $CB write	16
$CC	R	Reserved - $CC read	16
$CD		*reserved*	
$CE	W	Interrupt Mask - $CE write	16
$CF		*reserved*	

All other C-BUS addresses (including those not listed above) are either reserved for future use or allocated for production testing and must not be accessed in normal operation.

7.13.1 Interrupt Operation

The CMX7031/CMX7041 will issue an interrupt on the IRQN line when the IRQ bit (bit 15) of the Status register and the IRQ Mask bit (bit 15) are both set to 1. The IRQ bit is set when the state of the interrupt flag bits in the Status register change from a 0 to 1 and the corresponding mask bit(s) in the Interrupt Mask register is (are) set. Enabling an interrupt by setting a mask bit (0→1) after the corresponding Status register bit has already been set to 1 will also cause the IRQ bit to be set.

All interrupt flag bits in the Status register, except the Programming Flag (bit 0) and the RF Channel Status Flag (bit 1), are cleared and the interrupt request is cleared following the command/address phase of a C-BUS read of the Status register. The Programming Flag bit is set to 1 only when it is permissible to write a new word to the Programming register.

See:

- Status – $C6 read
- Interrupt Mask - $CE write

7.13.2 General Notes

In normal operation, the most significant registers are:

- Mode Control – $C1 write
- Status – $C6 read
- Input Gain and Routing - $B1 write
- Output Level – $C2 write

Setting the Mode register to either Rx or Tx will automatically increase the internal clock speed to its operational speed, whilst setting the Mode register to Idle will automatically return the internal clock to a lower (powersaving) speed. To access the Program Blocks (through the Programming register, $C8) the device MUST be in Idle mode.

8 Performance Specification

8.1 Electrical Performance

8.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

	Min.	Max.	Unit
Supply: DV_{DD}- DV_{SS}	–0.3	4.5	V
AV_{DD}- AV_{SS}	–0.3	4.5	V
RFV_{DD}- RFV_{SS}	–0.3	4.5	V
CPV_{DD}- RFV_{SS}	–0.3	4.5	V
Voltage on any pin to DV_{SS}	–0.3	DV_{DD} + 0.3	V
Voltage on any pin to AV_{SS}	–0.3	AV_{DD} + 0.3	V
Voltage on any pin to RFV_{SS} (excluding CPV_{DD})	–0.3	RFV_{DD} + 0.3	V
Current into or out of any power supply pin (excluding V_{BIAS}) (i.e. V_{DEC}, AV_{DD}, AV_{SS}, DV_{DD}, DV_{SS}, CPV_{DD}, RFV_{DD} or RFV_{SS})	–30	+30	mA
Current into or out of any other pin	–20	+20	mA
Voltage differential between power supplies:			
DV_{DD} and AV_{DD} or CPV_{DD}	0	0.3	V
AV_{DD} and CPV_{DD}	0	0.3	V
DV_{SS} and AV_{SS} or RFV_{SS}	0	50	mV
AV_{SS} and RFV_{SS}	0	50	mV

L9 Package (64-pin LQFP)	**Min.**	**Max.**	**Unit**
Total Allowable Power Dissipation at Tamb = 25°C	–	1690	mW
… Derating	–	16.9	mW/°C
Storage Temperature	–55	+125	°C
Operating Temperature	–40	+85	°C

Q1 Package (64-pin VQFN)	**Min.**	**Max.**	**Unit**
Total Allowable Power Dissipation at Tamb = 25°C	–	3500	mW
… Derating	–	35.0	mW/°C
Storage Temperature	–55	+125	°C
Operating Temperature	–40	+85	°C

L4 Package (48-pin LQFP)	**Min.**	**Max.**	**Unit**
Total Allowable Power Dissipation at Tamb = 25°C	–	1600	mW
... Derating	–	16.0	mW/°C
Storage Temperature	–55	+125	°C
Operating Temperature	–40	+85	°C

Q3 Package (48-pin VQFN)	**Min.**	**Max.**	**Unit**
Total Allowable Power Dissipation at Tamb = 25°C	–	1750	mW
... Derating	–	17.5	mW/°C
Storage Temperature	–55	+125	°C
Operating Temperature	–40	+85	°C

8.1.2 Operating Limits

Correct operation of the device outside these limits is not implied.

	Notes	Min.	Max.	Unit
Supply Voltage:				
DV_{DD} – DV_{SS}		3.0	3.6	V
AV_{DD} – AV_{SS}		3.0	3.6	V
CPV_{DD} – RFV_{SS}		3.0	3.6	V
RFV_{DD} – DV_{SS}	13	2.25	2.75	V
V_{DEC} – DV_{SS}	12	2.25	2.75	V
Operating Temperature		−40	+85	°C
XTAL/CLK Frequency (using an Xtal)	11	3.0	12.288	MHz
XTAL/CLK Frequency (using an external clock)	11	3.0	24.576	MHz

Notes

11 Nominal XTAL/CLK frequency is 19.2MHz.

12 The V_{DEC} supply is automatically created from DV_{DD} by the on-chip voltage regulator.

13 The RFV_{DD} supply can be supplied from the V_{DEC} supply, if preferred.

8.1.3 Operating Characteristics

For the following conditions unless otherwise specified:

External components as recommended in Figure 2 and Figure 3.
Maximum load on digital outputs = 30pF.
Osc Frequency = 19.2MHz ±0.01% (10ppm); Tamb = –40°C to +85°C.
AV_{DD} = DV_{DD} = CPV_{DD} = 3.0V to 3.6V; RFV_{DD} = 2.25V to 2.75V.
Reference Signal Level = 308mVrms at 1kHz with AV_{DD} = 3.3V.
Signal levels track with supply voltage, so scale accordingly.
Signal to Noise Ratio (SNR) in bit rate bandwidth.
Input stage gain = 0dB. Output stage attenuation = 0dB.

Current consumption figures quoted in this section apply to the device when loaded with 7031/7041FI-4.x only. The use of other Function Images™, can modify the current consumption of the device.

DC Parameters	Notes	Min.	Typ.	Max.	Unit
Supply Current	21				
All Powersaved					
DI_{DD} (DV_{DD} = 3.3V, V_{DEC} = 2.5V)		–	50	100	µA
AI_{DD} (AV_{DD} = 3.3V)		–	4	20	µA
CPI_{DD} + RFI_{DD} (CPV_{DD} = 3.3V, RFV_{DD} = 2.5V)		–	4	20	µA
IDLE Mode	22				
DI_{DD} (DV_{DD} = 3.3V, V_{DEC} = 2.5V)		–	TBD	–	mA
AI_{DD} (AV_{DD} = 3.3V)		–	TBD	–	µA
Rx Mode	22				
DI_{DD} (DV_{DD} = 3.3V, V_{DEC} = 2.5V)		–	TBD	–	mA
AI_{DD} (AV_{DD} = 3.3V)		–	TBD	–	mA
Tx Mode	22				
DI_{DD} (DV_{DD} = 3.3V, V_{DEC} = 2.5V)		–	TBD	–	mA
AI_{DD} (AV_{DD} = 3.3V)		–	TBD	–	mA
Additional Current for each RF Synthesiser	23				
CPI_{DD} + RFI_{DD} (CPV_{DD} = 3.3V, RFV_{DD} = 2.5V)		–		4.5	mA
Additional Current for each Auxiliary System Clock (output running at 4MHz)					
DI_{DD} (DV_{DD} = 3.3V, V_{DEC} = 2.5V)		–	500	–	µA
Additional Current for each Auxiliary ADC					
DI_{DD} (DV_{DD} = 3.3V, V_{DEC} = 2.5V)		–	5	–	µA
Additional Current for each Auxiliary DAC					
AI_{DD} (AV_{DD} = 3.3V)		–	200	–	µA

Notes:
21 Tamb = 25°C, Not including any current drawn from the device pins by external circuitry.
22 System Clocks, RF, Auxiliary circuits disabled, but all other digital circuits (including the Main Clock PLL) enabled.
23 When using the external components shown in Figure 16 and when supplying the current for RFV_{DD} from the regulated 2.5V digital (V_{DEC}) supply. The latter is derived from DV_{DD} by an on-chip voltage regulator.

DC Parameters (continued)	Notes	Min.	Typ.	Max.	Unit
XTAL/CLOCK	25				
Input Logic '1'		70%	–	–	DV_{DD}
Input Logic '0'		–	–	30%	DV_{DD}
Input Current (Vin = DV_{DD})		–	–	40	µA
Input Current (Vin = DV_{SS})		–40	–	–	µA
C-BUS Interface and Logic Inputs					
Input Logic '1'		70%	–	–	DV_{DD}
Input Logic '0'		–	–	30%	DV_{DD}
Input Leakage Current (Logic '1' or '0')	21	–1.0	–	1.0	µA
Input Capacitance		–	–	7.5	pF
C-BUS Interface and Logic Outputs					
Output Logic '1' (I_{OH} = 120µA)		90%	–	–	DV_{DD}
(I_{OH} = 1mA)		80%	–	–	DV_{DD}
Output Logic '0' (I_{OL} = 360µA)		–	–	10%	DV_{DD}
(I_{OL} = -1.5mA)		–	–	15%	DV_{DD}
"Off" State Leakage Current	21	–	–	10	µA
IRQN (Vout = DV_{DD})		–1.0	–	+1.0	µA
RDATA (output HiZ)		–1.0	–	+1.0	µA
V_{BIAS}	26				
Output Voltage Offset wrt $AV_{DD}/2$ (I_{OL} < 1µA)		–	±2%	–	AV_{DD}
Output Impedance		–	22	–	kΩ

Notes: 25 Characteristics when driving the XTAL/CLOCK pin with an external clock source.

26 Applies when utilising V_{BIAS} to provide a reference voltage to other parts of the system. When using V_{BIAS} as a reference, V_{BIAS} must be buffered. V_{BIAS} must always be decoupled with a capacitor as shown in Figure 2 and Figure 3.

AC Parameters		Notes	Min.	Typ.	Max.	Unit
XTAL/CLOCK Input						
'High' Pulse Width		31	15	–	–	ns
'Low' Pulse Width		31	15	–	–	ns
Input Impedance (at 6.144MHz)						
Powered-up	Resistance		–	150	–	kΩ
	Capacitance		–	20	–	pF
Powered-down	Resistance		–	300	–	kΩ
	Capacitance		–	20	–	pF
Xtal Start-up Time (from powersave)			–	20	–	ms
Auxiliary SYSCLK1/2 Outputs						
XTAL/CLK Input to CLOCK_OUT Timing:						
(in high to out high)		32	–	15	–	ns
(in low to out low)		32	–	15	–	ns
'High' Pulse Width		33	76	81.38	87	ns
'Low' Pulse Width		33	76	81.38	87	ns
V_{BIAS}						
Start-up Time (from powersave)			–	30	–	ms
MIC, ALT, DISC Inputs						
Input Impedance		34	–	1	–	MΩ
Maximum Input Level (pk-pk)		35	–	–	80%	AV_{DD}
Load Resistance (feedback pins)			80	–	–	kΩ
Amplifier Open Loop Voltage Gain (I/P = 1mVrms at 100Hz)			–	60	–	dB
Unity Gain Bandwidth			–	1.0	–	MHz
Input 1 Gain Stage		36				
Gain (at 0dB)		37	−0.5	0	+0.5	dB
Cumulative Gain Error (wrt attenuation at 0dB)		37	−1.0	0	+1.0	dB

Notes:

31 Timing for an external input to the XTAL/CLOCK pin.

32 XTAL/CLOCK input driven by an external source.

33 19.2MHz oscillator.

34 With no external components connected.

35 Centred about $AV_{DD}/2$; after multiplying by the gain of input circuit (with external components connected).

36 Gain applied to signal at output of buffer amplifier: DISCFB, ALTFB OR MICFB.

37 Design Value. Overall attenuation input to output has a tolerance of 0dB ±1.0dB.

AC Parameters	Notes	Min.	Typ.	Max.	Unit
MOD 1 and MOD2					
Power-up to Outputs Stable	41	–	50	100	µs
Attenuation (at 0dB)	43	–1.0	0	+1.0	dB
Cumulative Attenuation Error (wrt attenuation at 0dB)		–0.6	0	+0.6	dB
Output Impedance Enabled	42	–	600	–	Ω
Output Impedance Disabled	42	–	500	–	kΩ
Output Current Range (AV_{DD} = 3.3V)		–	–	±125	µA
Output Voltage Range	44	0.5	–	AV_{DD} –0.5	V
Load Resistance		20	–	–	kΩ

Notes:

41 Power-up refers to issuing a C-BUS command to turn on an output. These limits apply only if V_{BIAS} is on and stable. At power supply switch-on, the default state is for all blocks, except the XTAL and C-BUS interface, to be in placed in powersave mode.

42 Small signal impedance, at AV_{DD} = 3.3V and Tamb = 25°C.

43 With respect to the signal at the feedback pin of the selected input port.

44 Centred about $AV_{DD}/2$; with respect to the output driving a 20kΩ load to $AV_{DD}/2$.

AC Parameters (cont.)	Notes	Min.	Typ.	Max.	Unit
Auxiliary Signal Inputs (Aux ADC 1 to 4)					
Source Output Impedance	51	–	–	24	kΩ
Auxiliary 10 Bit ADCs					
Resolution		–	10	–	Bits
Maximum Input Level (pk-pk)	54	–	–	80%	AV_{DD}
Conversion Time	52	–	250	–	µs
Input Impedance					
Resistance		–	10	–	MΩ
Capacitance		–	5	–	pF
Zero Error (input offset to give ADC output = 0)		0	–	±10	mV
Integral Non-linearity		–	–	±3	LSBs
Differential Non-linearity	53	–	–	±1	LSBs
Auxiliary 10 Bit DACs					
Resolution		–	10	–	Bits
Maximum Output Level (pk-pk), no load	54	80%	–	–	AV_{DD}
Zero Error (output offset from a DAC input = 0)		0	–	±10	mV
Resistive Load		5	–	–	kΩ
Integral Non-linearity		–	–	±4	LSBs
Differential Non-linearity	53	–	–	±1	LSBs

Notes:

51 Denotes output impedance of the driver of the auxiliary input signal, to ensure < 1 bit additional error under nominal conditions.

52 With an auxiliary clock frequency of 6.144MHz.

53 Guaranteed monotonic with no missing codes.

54 Centred about $AV_{DD}/2$.

AC Parameters (cont.)	Notes	Min.	Typ.	Max.	Unit
RF Synthesisers – Phase Locked Loops					
Reference Clock Input					
Input Logic '1'	62	70%	–	–	RFV_{DD}
Input Logic '0'	62	–	–	30%	RFV_{DD}
Frequency	64,66	5.0	19.2	40.0	MHz
Divide Ratios (R)	63	2	–	8191	
Each RF Synthesiser	69				
Comparison Frequency		–	–	500	kHz
Input Frequency Range	67	100	–	600	MHz
Input Level		−14	–	0	dBm
Input Slew Rate		14	–	–	V/µs
Divide Ratios (N)		1088	–	1048575	
1Hz Normalised Phase Noise Floor	68	–	−197	–	dBc/Hz
Charge Pump Current (high)	65	±1.88	±2.5	±3.3	mA
Charge Pump Current (low)	65	±470	±625	±820	µA
Charge Pump Current – voltage variation		–	10%	–	per V
Charge Pump Current – sink to source match		–	5%	–	of ISET

Notes:

62 Square wave input.

63 Separate dividers are provided for each PLL.

64 For optimum performance of the synthesiser subsystems, a common master clock should be used for the RF Synthesisers and the baseband sections. Using unsynchronised clocks is likely to result in spurious products being generated in the synthesiser outputs and in some cases difficulty may be experienced in obtaining lock in the RF Synthesisers.

65 External ISET resistor (R31) = 0Ω (Internal ISET resistor = 9k6Ω nominally).

66 Lower input frequencies may be used subject to division ratio requirements being maintained.

67 Operation outside these frequency limits is possible, but not guaranteed. Below 150MHz, a square wave input may be required to provide a fast enough slew rate.

68 1Hz Normalised Phase Noise Floor (PN1Hz) can be used to calculate the phase noise within the PLL loop by:

Phase Noise (in-band) = $PN1Hz + 20\log_{10}(N) + 10\log_{10}(f_{comparison})$.

69 It is recommended that RF Synthesiser 1 be used for the higher frequency use (eg: RF 1st LO) and RF Synthesiser 2 be used for lower frequency use (eg: IF LO).

8.1.4 Parametric Performance

For the following conditions unless otherwise specified:

External components as recommended in Figure 2 and Figure 3.
Maximum load on digital outputs = 30pF.
Osc Frequency = 19.2MHz ±0.01% (10ppm)); Tamb = –40°C to +85°C.
AV_{DD} = DV_{DD} = CPV_{DD} = 3.0V to 3.6V; RFV_{DD} = 2.25V to 2.75V.
Reference Signal Level = 308mVrms at 1kHz with AV_{DD} = 3.3V.
Signal levels track with supply voltage, so scale accordingly.
Signal to Noise Ratio (SNR) in bit rate bandwidth.
Input stage gain = 0dB, Output stage attenuation = 0dB.

All figures quoted in this section apply to the device when loaded with FI4.x only. The use of other Function Images™, can modify the parametric performance of the device.

AC Parameters (cont.)		Notes	Min.	Typ.	Max.	Unit
Receiver Signal Type Identification						
Probability of correctly identifying signal type (SNR = 12dB)			–	>>99.9	–	%
GMSK Decoder						
Signal Input Dynamic Range		74	100	–	800	mVrms
Bit Error Rate	(SNR = 20dB)	74	–	TBD	–	10^{-8}
Receiver Synchronisation	(SNR = 12dB)			TBD		
AFSK Decoder						
Signal Input Dynamic Range		74	100	–	800	mVrms
Bit Error Rate	(SNR = 20dB)	74	–	TBD	–	10^{-8}
Receiver Synchronisation	(SNR = 12dB)			TBD		

Notes:

74 AV_{DD} = 3.3V, for a “101010101 … 01” pattern measured at the input amplifier feedback pin. Signal level scales with AV_{DD}.

AC Parameters (cont.)	Notes	Min.	Typ.	Max.	Unit
DTMF Encoder					
Output Signal Level		–	360	775	mVrms
Output Level Variation			0.5		dB
Output Distortion		–	–	5	%
GMSK Encoder					
Output Signal Level		–	775	–	mVrms
Output Level Variation		−1.0	0	+1.0	dB
Output Distortion		–	–	5	%
3rd Harmonic Distortion		–	–	3	%
Filter Bt			0.5		
AFSK Encoder					
Output Signal Level		–	775	–	mVrms
Output Level Variation		−1.0	0	+1.0	dB
Output Distortion		–	–	5	%
3rd Harmonic Distortion		–	–	3	%
Logic 1 Frequency		1198	1200	1202	Hz
Logic 0 Frequency		2118	2200	2202	Hz
Isochronous Distortion (0 to 1 and 1 to 0)		–	–	40	µs

Notes:
81 AV_{DD} = 3.3V.
82 Measured at MOD 1 or MOD 2 output.
83 AV_{DD} = 3.3V and Tx Audio Level set to 871mV p-p (308mVrms).
84 AV_{DD} = 3.3V.

8.2 C-BUS Timing

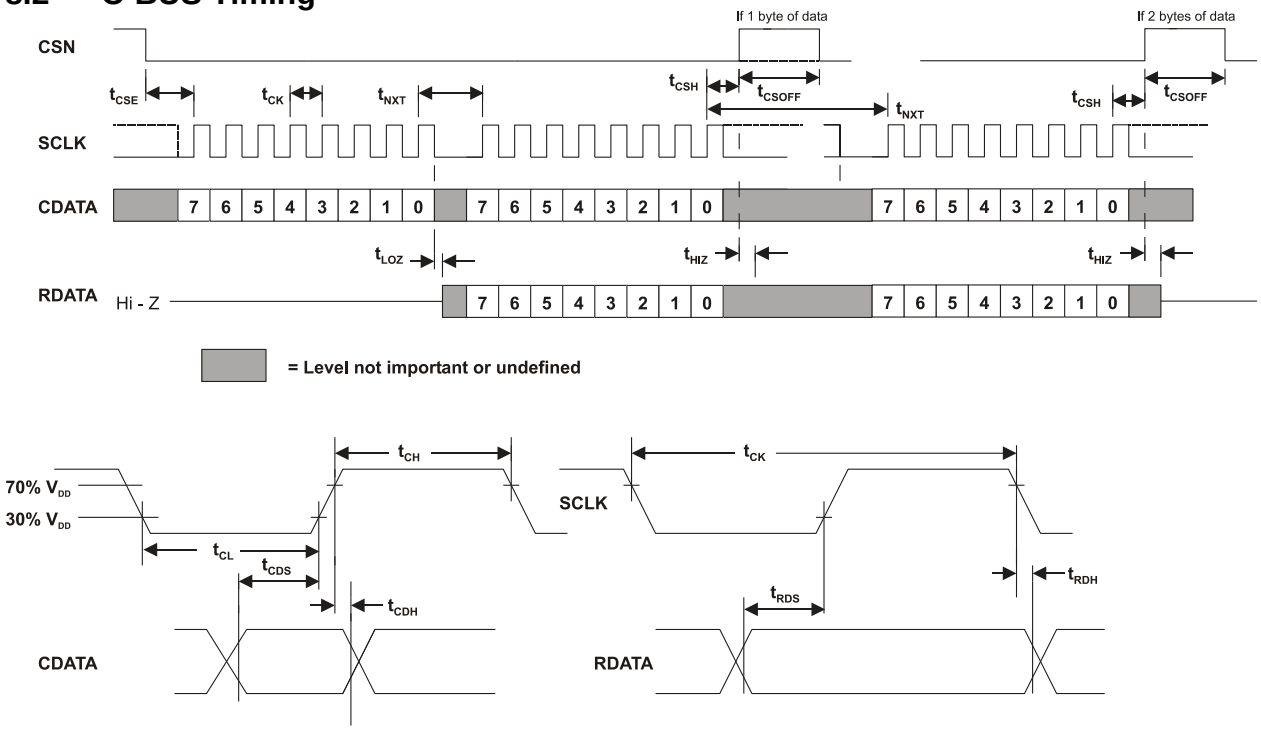


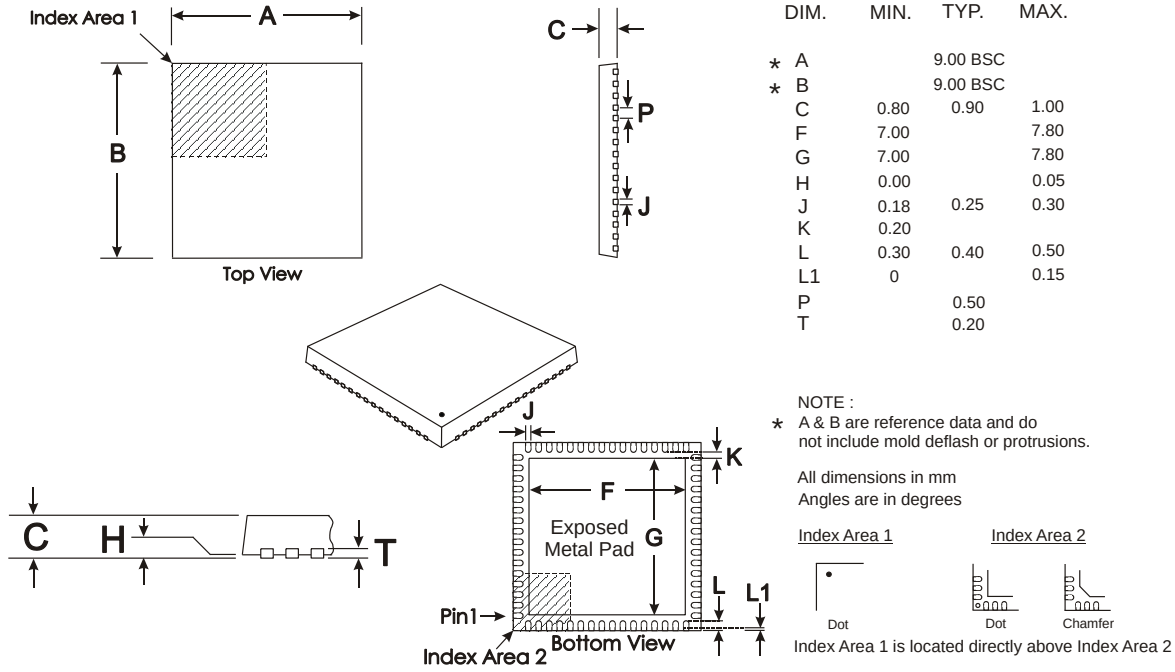
Figure 20 C-BUS Timing

C-BUS Timing		Notes	Min.	Typ.	Max.	Unit
t_{CSE}	CSN Enable to SCLK high time		100	–	–	ns
t_{CSH}	Last SCLK high to CSN high time		100	–	–	ns
t_{LOZ}	SCLK low to RDATA Output Enable time		0.0	–	–	ns
t_{HIZ}	CSN high to RDATA high impedance		–	–	1.0	µs
t_{CSOFF}	CSN high time between transactions		1.0	–	–	µs
t_{NXT}	Inter-byte time		200	–	–	ns
t_{CK}	SCLK cycle time		200	–	–	ns
t_{CH}	SCLK high time		100	–	–	ns
t_{CL}	SCLK low time		100	–	–	ns
t_{CDS}	CDATA setup time		75	–	–	ns
t_{CDH}	CDATA hold time		25	–	–	ns
t_{RDS}	RDATA setup time		50	–	–	ns
t_{RDH}	RDATA hold time		0	–	–	ns

Notes:
1. Depending on the command, 1 or 2 bytes of CDATA are transmitted to the peripheral MSB (Bit 7) first, LSB (Bit 0) last. RDATA is read from the peripheral MSB (Bit 7) first, LSB (Bit 0) last.
2. Data is clocked into the peripheral on the rising SCLK edge.
3. Commands are acted upon at the end of each command (rising edge of CSN).
4. To allow for differing µC serial interface formats C-BUS compatible ICs are able to work with SCLK pulses starting and ending at either polarity.
5. Maximum 30pF load on IRQN pin and each C-BUS interface line.

These timings are for the latest version of C-BUS and allow faster transfers than the original C-BUS timing specification. The CMX7031/CMX7041 can be used in conjunction with devices that comply with the slower timings, subject to system throughput constraints.

8.3 Packaging



DIM.	MIN.	TYP.	MAX.
* A		9.00 BSC	
* B		9.00 BSC	
C	0.80	0.90	1.00
F	7.00		7.80
G	7.00		7.80
H	0.00		0.05
J	0.18	0.25	0.30
K	0.20		
L	0.30	0.40	0.50
L1	0		0.15
P		0.50	
T		0.20	

NOTE :
* A & B are reference data and do not include mold deflash or protrusions.

All dimensions in mm
Angles are in degrees

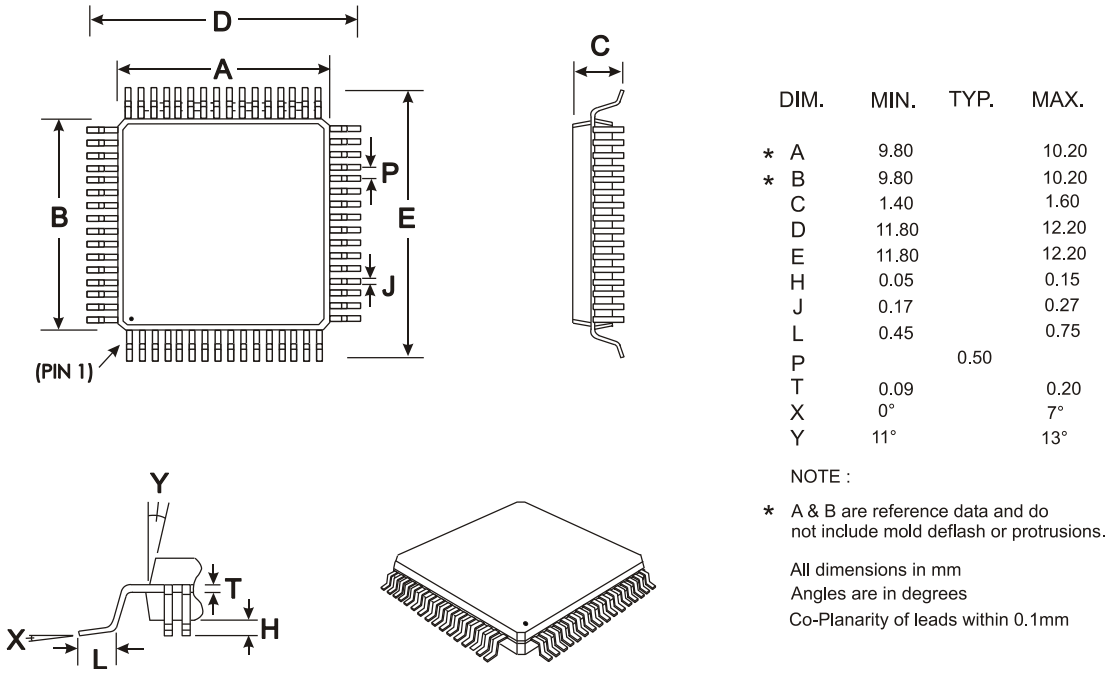
Index Area 1 Index Area 2

Index Area 1 is located directly above Index Area 2

Depending on the method of lead termination at the edge of the package, pull back (L1) may be present.
L minus L1 to be equal to, or greater than 0.3mm
The underside of the package has an exposed metal pad which should ideally be soldered to the pcb to enhance the thermal conductivity and mechanical strength of the package fixing. Where advised, an electrical connection to this metal pad may also be required

Figure 21 Mechanical Outline of 64-pin VQFN (Q1)

Order as part no. CMX7031Q1



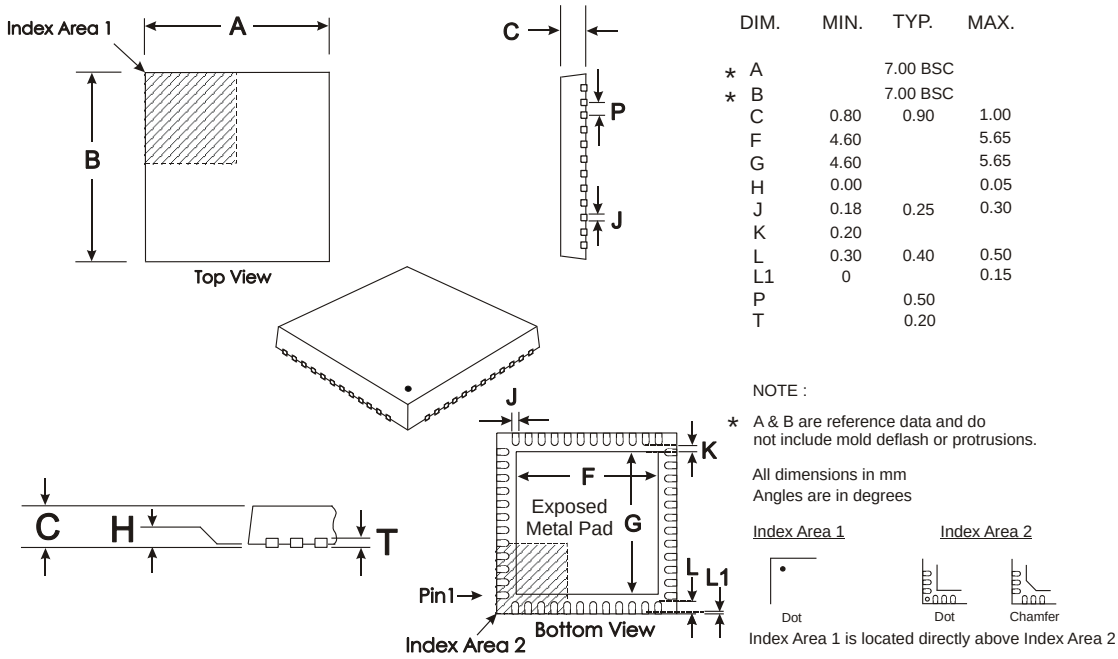
DIM.	MIN.	TYP.	MAX.
* A	9.80		10.20
* B	9.80		10.20
C	1.40		1.60
D	11.80		12.20
E	11.80		12.20
H	0.05		0.15
J	0.17		0.27
L	0.45		0.75
P		0.50	
T	0.09		0.20
X	0°		7°
Y	11°		13°

NOTE :
* A & B are reference data and do not include mold deflash or protrusions.

All dimensions in mm
Angles are in degrees
Co-Planarity of leads within 0.1mm

Figure 22 Mechanical Outline of 64-pin LQFP (L9)

Order as part no. CMX7031L9



DIM.	MIN.	TYP.	MAX.
* A		7.00 BSC	
* B		7.00 BSC	
C	0.80	0.90	1.00
F	4.60		5.65
G	4.60		5.65
H	0.00		0.05
J	0.18	0.25	0.30
K	0.20		
L	0.30	0.40	0.50
L1	0		0.15
P		0.50	
T		0.20	

NOTE :

* A & B are reference data and do not include mold deflash or protrusions.

All dimensions in mm
Angles are in degrees

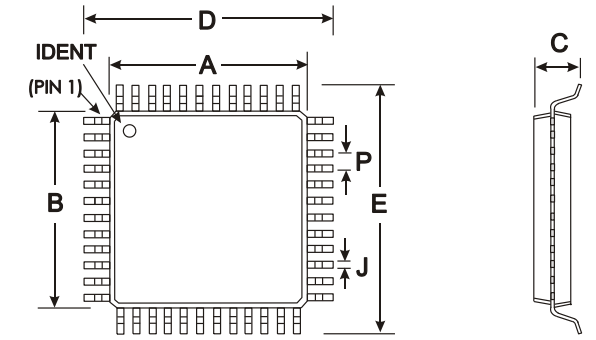
Index Area 1 Index Area 2

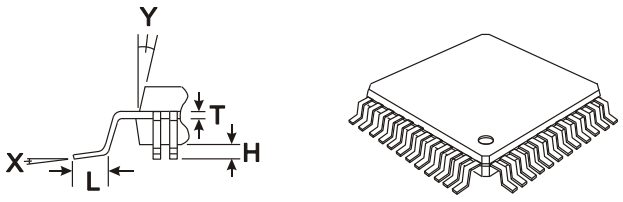
Index Area 1 is located directly above Index Area 2

Depending on the method of lead termination at the edge of the package, pull back (L1) may be present.
L minus L1 to be equal to, or greater than 0.3mm
The underside of the package has an exposed metal pad which should ideally be soldered to the pcb to enhance the thermal conductivity and mechanical strength of the package fixing. Where advised, an electrical connection to this metal pad may also be required

Figure 23 Mechanical Outline of 48-pin VQFN (Q3)

Order as part no. CMX7041Q3





DIM.	MIN.	TYP.	MAX.
* A	6.91		7.11
* B	6.91		7.11
C	1.40		1.60
D	8.74		9.25
E	8.74		9.25
H	0.05		0.15
J	0.10		0.28
L	0.35		0.76
P		0.50	
T		0.13	
X	0°		7°
Y	11°		13°

NOTE :

* A & B are reference data and do not include mold deflash or protrusions.

All dimensions in mm
Angles are in degrees
Co-Planarity of leads within 0.1mm

Figure 24 Mechanical Outline of 48-pin LQFP (L4)

Order as part no. CMX7041L4

As package dimensions may change after publication of this datasheet, it is recommended that you check for the latest Packaging Information from the Design Support area of the CML website: [http://www.cmlmicro.com/].

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